



SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY

Thirupachur-631203, Thiruvallur TK& DT.
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai
Academic Calendar- 2022-2023

ACADEMIC CALENDAR- EVEN SEMESTER (II, III & IV Year) 2022-2023

DAY	CWD	DATE	Jan-22			Feb/23			Mar/23			Apr/23			May/23		
			CWD	DATE		CWD	DATE		CWD	DATE		CWD	DATE		CWD	DATE	
MON		2														67	1
TUE		3														68	2
WED		4							27	1						69	3
THU		5							28	2						70	4
FRI		6							29	3						71	5
SAT		7	HOLIDAY		8	4	Zeroth Project Review		4	HOLIDAY		1	HOLIDAY			6	HOLIDAY
SUN		8	HOLIDAY			5	HOLIDAY		5	HOLIDAY		2	HOLIDAY			7	HOLIDAY
MON		9			9	6	Int Asst -I / Final year	30	6		49	3	Third Project Review			72	8
TUE		10			10	7	Int Asst -I / Final year	31	7		50	4				73	9
WED		11			11	8		32	8		51	5				74	10
THU		12			12	9		33	9		52	6				75	11
FRI		13	Pongal Holidays		13	10		34	10			7	Good Friday			76	12
SAT		14	Pongal Holidays		14	11			11	HOLIDAY		8	HOLIDAY			13	HOLIDAY
SUN		15	Pongal Holidays		15	12	HOLIDAY		12	HOLIDAY		9	HOLIDAY			14	HOLIDAY
MON		16	Pongal Holidays		15	13	II/III Year Reopens	35	13	Model Exam / Int Asst -I	53	10				77	15
TUE		17	Pongal Holidays		16	14	Int Asst -II / Final year	36	14	Model Exam / Int Asst -I	54	11				78	16
WED		18	Pongal Holidays		17	15	Int Asst -II / Final year	37	15	Second Review / Int Asst -I	55	12				79	17
THU		19			18	16		38	16	Int Asst -I	56	13				80	18
FRI		20			19	17		39	17	Int Asst -I		14	Tamil New Year			19	Practicals
SAT		21	HOLIDAY			18	HOLIDAY		18	HOLIDAY		15	HOLIDAY			20	HOLIDAY
SUN		22	HOLIDAY			19	HOLIDAY		19	HOLIDAY		16	HOLIDAY			21	HOLIDAY
MON		23			20	20		40	20	Int Asst -I	57	17	Int Asst -II			22	Practicals
TUE		24			21	21		41	21		58	18	Int Asst -II			23	Practicals
WED		25			22	22			22	Telugu New Year	59	19	Int Asst -II			24	Practicals
THU		26	Republic Day		23	23		42	23		60	20	Int Asst -II			25	Practicals
FRI	1	27	Final Year Reopens		24	24		43	24		61	21	Int Asst -II			26	Theory Starts
SAT	2	28				25	HOLIDAY		25	HOLIDAY		22	Ramzan			27	HOLIDAY
SUN		29	HOLIDAY			26	HOLIDAY		26	HOLIDAY		23	HOLIDAY			28	HOLIDAY
MON	3	30			25	27		44	27		62	24	Int Asst -II			29	
TUE	4	31			26	28	First Project Review	45	28		63	25				30	
WED								46	29		64	26				31	
THU								47	30		65	27					
THU								48	31		66	28					
FRI												29	HOLIDAY				
SAT												30	HOLIDAY				
SUN																	



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MECHANISM OF INTERNAL/ EXTERNAL ASSESSMENT IS TRANSPARENT AND THE GRIEVANCE REDRESSAL SYSTEM IS TIME- BOUND AND EFFICIENT.

INTERNAL ASSESSMENT MECHANISM

The Internal Assessment Mechanism of an Educational Institution Plays a Crucial Role in Evaluating the Academic Performance of Students.

- The Internal Assessment Mechanism Comprises Two Continuous Internal Assessment Tests And A Model Examination.
- The Tests Are 1.5 Hours Long And Carry A Weightage Of 50 Marks, While The Model Examination Is 3 Hours Long And Carries A Weightage Of 100 Marks.
- The Schedule For These Assessments Is Set By The Affiliating University And Is Made Available To Students Via The Academic Calendar, Notice Boards, And Other Communication Channels.

QUESTION PAPER SETTING AND CORRECTION

The Format Of The Question Paper And Syllabus For These Assessments Is Discussed In The Classroom, Ensuring That Students Are Well-Prepared. Furthermore, The Question Papers Are Verified By The Internal Quality Assurance Cell (IQAC) Coordinator And The Head Of The Department (HOD) To Identify And Rectify Any Errors Or Ambiguities In The Questions.

The Faculty Prepares The Answer Key For The Assessments Along With The Mark Allocation, Which Is Displayed On The Notice Board For The Benefit Of Students. The Corrected Answer Scripts Are Returned To Students Within Two Working Days, And Any Deviations In The Awarding Of Marks Are Rectified By The Faculty. The Mark Lists Are Also Sent To Parents By Post To Ensure Transparency. In Cases Where A Student Is Unable To Attend The Assessments Due To Medical Grounds Or Other Valid Reasons With Prior Permissions, A Retest Is Conducted.


EXTERNAL ASSESSMENT MECHANISM

If A Student Is Not Satisfied With The End Semester Exam Results Published By The University, They Can Request A Photocopy Of The Evaluated Answer Script. If A Student Is Still Not Satisfied With The Awarded Marks, They Can Apply For Reassessment Of The Answer Script After Consulting With The Faculty Member. If The Student Is Still Not Satisfied With The Second Assessment, They Can Apply For A Challenging Valuation.

GRIEVANCE REDRESSAL SYSTEM

To Ensure That The Grievances Of Students Are Addressed In A Timely And Effective Manner, A Grievance Redressal Committee Is In Place. The Committee Is Made Up Of The Principal, Dean, And HOD. The Cell Provides A Platform For Students To Express General And Personal Grievances, Through Various Channels Such As Mentor-Mentee Meetings, Class Committee Meetings, Suggestion Boxes, And Feedback From Parents.




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CONTINUOUS PERFORMANCE MONITORING

Mentor-Mentee Meetings Are Conducted Twice A Month and Consist Of 10 To 15 Students per Faculty Member. Class Committee Meetings Are Conducted Thrice A Semester And Comprise A Chairperson From Another Department, Members Of The Subject Handling Faculty, And Six Students From The Class. These Meetings Are Student-Centric And Allow Students To Express Their Grievances Before The Chairperson And Committee Members. Results Are Analyzed Periodically To Segment Students Accordingly And Provide Meaningful Feedback To Students Across Different Score Percentiles.

Suggestion Boxes Are Placed At Various Locations Throughout The Institution And Opened Once A Week. All Relevant Suggestions From Different Channels Such As Suggestion Box, Parent-Teacher Meetings, Result Analysis And Grievance Redressal System Are Conveyed To The Management For Expedited Action.




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EXAMINATION CELL

The Examination Cell, led by the principal serving as the Chief Superintendent of Examinations, along with a team of assistants, plays a crucial role in overseeing the assessment process at TIET. Its primary duty involves administering all examinations, internal and external, with adherence to fairness, thoroughness, and compliance with directives from the Chief Superintendent of Examinations.

GOAL

Ensure all tasks related to internal and external assessments are completed in accordance with university policies and announcements.

FUNCTION OF EXAM CELL

The examination cell processes notifications, office orders, guidelines, circulars, and notices received by the college. After being signed by the principal, they are forwarded to the university as responses.

ANALYSIS

- The University ensures timely forwarding of notices to all relevant parties. These notices contain information such as fine payment procedures, fee deadlines, and other pertinent details. The Examination Cell is responsible for overseeing both internal and university examinations across all undergraduate (UG) and postgraduate (PG) programs.
- Arranging the timetable, the assignment of seats in the examination halls, the invigilation duty chart, and other details necessary for a seamless examination process. During the examination period, appropriate staff mobilization and assignment of duties in accordance with the previously prepared duty chart. Following the exam's completion, the answer books are given to the relevant teachers, the answer books and award list are received, and they are prepared in the required format before being sent to the university. All examination results are analyzed by the Examination cell, and after consulting with the Principal Give the concerned department instructions to compile the report so that it can be sent to the proper authorities for follow up

GRIEVANCES RELATED TO INTERNAL ASSESSMENT

- A student's examination is conducted in accordance with protocol if they are unable to appear for an internal exam for any legitimate reason, such as a medical condition, as long as they send a letter to the department head along with the necessary paperwork
- The assessment report is prepared and presented to the students; in the event that any complaints are there, it can be promptly resolved and submitted to the department by the faculty member in question. Students who wish to improve in a particular subject and receive lower marks can take the improvement exam or turn in an improvement assignment. Student complaints about assessments are clarified by displaying their performance on the response sheet




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- In the presence of the student, the faculty members reevaluate the student's response sheet. Faculty members promptly rectify any discrepancies in the final grade or answer book evaluation that students have pointed out. Any student who is unhappy with the evaluation and mark distribution can speak with the concerned HOD, who can step in and get the input of another course instructor.

GRIEVANCES CONNECTED WITH THE END-SEMESTER UNIVERSITY EXAMINATION

- The Chief Examination Officer promptly communicates with the principal to resolve any issues related to inaccuracies in names, courses, and programs on hall passes and mark sheets, as well as complaints regarding difficulties with test form submissions.
- Any grievances concerning university question papers, including topics not covered in the syllabus, repeated questions, incorrect distribution of marks, missed marks, or Mis -numbered questions during semester exams, should be reported to the principal. Subsequently, the principal will promptly review the daily university question papers alongside the department head and subject faculty members, and then take appropriate action by communicating with the university.
- Faculty members assess the difficulty percentage of question papers and provide feedback to the department head. Upon the university's decision or receipt of information through the principal, relevant departments are promptly notified of the grievance resolution process. Subject-matter experts and class counselors then communicate this to students. Should a student receive a grade lower than expected in their university examination, they have the option to request a reevaluation of their answer script by paying the necessary fee. The university provides students with photocopies of their answer sheets in case of evaluation complaints. If a student finds the evaluation to be inaccurate, they may request a reevaluation. Furthermore, students can opt for challenge reevaluation if they still have grievances post-discussion with the department head and subject-handling faculty.



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EXAMINATION – ASSESSMENT POLICY

The College Follows Internal and External Assessment as Per Anna University Norms, Following As Pattern of Assessment (2021 Regulation)

INTERNAL EXAMINATION	40 %
EXTERNAL EXAMINATION	60 %


I. CONDUCT OF INTERNAL ASSESSMENT EXAMINATION

- The main objective of internal assessment is to regularly evaluate the knowledge and skills students have gained. This is achieved through a variety of methods such as internal assessment exams, daily slip tests in class, homework assignments, projects, oral exams, presentations, group discussions, and practical assessments.
- The provisional timetable for internal assessment exams is indicated in the College Academic Calendar.
- The college conducts three internal assessments (I, II, and III) for each course prior to the commencement of each program.
- Attendance for internal assessment is compulsory.
- The Controller of Examination, in consultation with the Principal and Heads of Departments, establishes the specific schedules. Circulars are circulated in advance to inform both staff and students of these schedules. Portions for Internal Assessment Tests are divided based on syllabus units completed, as follows:

Internal Assessment	Portions	Marks
Internal Assessment - I	Unit I & II	100
Internal Assessment - II	Unit III & IV	100
Model Examination	All 5 units (I, II, III, IV, V)	100

- The department exam cell members notify and instructs the subjects handling faculty to prepare the university pattern question paper and submit the printed copy to the examination cell by the deadline stated in the circular.
- The exam cell sets up the seating and hall arrangements.
- The exam cell created a schedule for invigilation duty.
- a squad committee is established to keep as eye on the designated examination hall report to the principal and exam cell every day.
- Answer sheets and the attendance report are collected by the invigilated and given to the exam cell following exam. Through department exam cell members, the subject handling faculty receives the answer sheets from exam cell.
- Following Evaluation Student Receive Their Answer Paper Along with Comments for Improvement and Their Marks, Each Student's Specific Are Document. The Mark List Is Sent the Class Counselors, Who Compile the Data from Each Class and Forward It to The Exam Cell for Internal Examination.




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PRACTICAL SUBJECTS

MODEL PRACTICAL EXAMINATIONS

- Before the final week of classes (according to the schedule provided by the relevant departments), students must complete all lab manuals, document their work, and acquire signatures from the appropriate staff members to qualify for participation in the model practical examinations.


PROCEDURES FOR AWARDING MARKS IN INTERNAL ASSESSMENT

- Each faculty member must maintain a logbook containing attendance records for every lecture, practical, or project session, along with test scores and classwork details (including topics covered) for each subject. This logbook should be submitted to the Head of the Department and Principal for review to ensure syllabus coverage and accuracy of test marks and attendance records.
- After due verification, the Head of the Department will sign the logbook and then submit it to the principal for their signature along with the date.
- Upon the conclusion of the semester, the record should undergo verification by the Head of the Institution, who will then securely store this document for a period of five years.
- The university or any inspection team designated by the University has the authority to review the records of attendance and assessment from both the current and past semesters.
- The Examination Cell gathers internal marks from different departments and submits them to the University according to the University's prescribed format prior to the commencement of University Examinations.

CONDUCT OF END SEMESTER UNIVERSITY EXAMINATION

- During both odd and even semesters, the end-of-semester exams are conducted according to the schedule provided by Anna University.
The Exam Cell arranges the examination hall and seating arrangements according to the format specified by the university. Upon entering the examination hall, candidates are responsible for locating their designated hall and seat, identifying their register numbers, and occupying their assigned seats. The University examinations are conducted according to the specified timings as per Anna University guidelines.




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UNIVERSITY SCHEDULED

- The Hall Superintendent distributes both the answer booklets and the question papers.
- Upon finishing the examination, students submit their answer booklets to the Hall Superintendent. The Hall Superintendent then collects and organizes them in sequential order, either by branch or register number, and delivers them to the COE/Chief Superintendent.
- The answer booklets handed over by the Hall Superintendent are kept in sealed covers with endorsement by Chief Superintendent and University Representative.
- The Chief Superintendent, through the University Representative, delivers the sealed covers to the Zonal office.
- The Hall Superintendent informs the COE/Chief Superintendent of any instances of malpractice by candidates during the examination.
- The Chief Superintendent forwards it to the university along with a cover letter, a seating chart for students, and reports from the hall superintendent.
- The University determines any necessary disciplinary actions and informs the respective student and principal of the decision. Subsequently, the Principal notifies the relevant Head of Department (HOD).



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Dr. S. Palani ME. Ph.d
Principal

CERTIFICATE


This is certified that the constitution of Internal & External exam cell committee for the academic year 2022 - 2023 is given below.

INTERNAL EXAM CELL COMMITTEE

The Internal examination cell is constituted for the academic year 2022 – 2023 with the following Members.

<i>S.NO</i>	<i>NAME OF THE FACULTY</i>	<i>DESIGNATION</i>	<i>ROLE</i>
1	Dr. S. Palani	Principal	Convener
2	Mr. D.Babu	Assistant Professor / MBA	Chief Co - ordinated
3	Mrs.P.Kanimozhi	Assistant Professor / MCA	Member
4	Ms.J.Sangeetha	Assistant Professor / CSE	Member
5	Mr. V.Rajesh Kumar	Assistant Professor / ECE	Member
6	Mrs.S.Geetha	Assistant Professor / EEE	Member
7	Mr. V.Varun Kumart	Assistant Professor / CIVIL	Member
8	Mr. Vinoth	Assistant Professor / MECH	Member
9	Mr. Ragavendran	Assistant Professor / S & H	Member




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UNIVERSITY EXAM CELL COMMITTEE

The External examination cell is constituted for the academic year 2023 – 2024 with the following Members.

<i>S.NO</i>	<i>NAME OF THE FACULTY</i>	<i>DESIGNATION</i>	<i>ROLE</i>
1	Dr. S. Palani	Principal	Principal / Chief Superintendent
2	Mr. D. Babu	Assistant Professor / MBA	Chief exam cell Co - ordinated
3	Mr. Sundaram	System Engineer	System Engineer




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INTERNAL & EXTERNAL EXAMINATION GRIEVANCES REDRESSAL CELL (SVCET)

Internal & External Examination Grievances Redressal is constituted for the Academic year
2023 – 2024 with the following member

S.NO	NAME OF THE FACULTY	DESIGNATION	E-MAIL ID & CONTACT NUMBER
1	Dr. S. Palani	Principal	palaniraji.s@gmail.com 94443653965
2	Mr. D. Babu	Assistant Professor / MBA – HOD	babulib2004@gmail.com 9444134702
3	Mrs.N.Jayakumari	Assistant Professor / MCA – HOD	Jayanarayana.90@gmail.com 9994550528
4	Ms.J.Sangeetha	Assistant Professor / CSE – HOD	Sangeeparthi143@gmail.com 8754995324
5	Mr. V. Rajesh Kumar	Assistant Professor / ECE – HOD	v.rajeshdevan11@gmail.com 9677204739
6	Mr.M.Namachivayam	Assistant Professor / EEE – HOD	Namachu30@gmail.com 9940269316
7	Mr. V.Varun Kumar	Assistant Professor / CIVIL – HOD	varunstructural@gmail.com 9789391957
8	Mr. M.Vinoth	Assistant Professor / MECH – HOD	vinoth.m02@gmail.com 9894971302
9	Mr. S.Ragavendran	Assistant Professor / S & H – HOD	ragavendran1981@gmail.com 7358011921




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INTERNAL TEST CIRCULAR



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CIRCULAR

All The HOD Are Hereby Informed To Complete The Assessment Test – 1 For UG Students Between (1ST YEAR) And Also Submit 2 Set Of Question Paper To The Exam Cell On Or Before (23.6.2023) 12: 00, Allocation Of Marks For The Assessment Test Should Be As Prescribed Below.

Regulation – 2021

Part – A -----→ 7 X 2 = 14 (With Choice)
Part – B -----→ 2 X 13 = 26 (With Choice)
Part – C -----→ 1 X 10 = 10 (With Choice)
Total -----→ 50 Marks


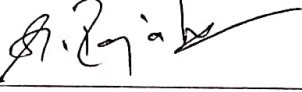

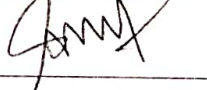


Exam Coordinator





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Copy To

- 1) The Management for kind information
- 2) All department HODs, Faculties & Students.
- 3) Department Notice Boards
- 4) Office & file

S. NO	DEPARTMENT	HOD SIGN
1	CIVIL	
2	MECH	
3	CSE	
4	ELECTRICAL	
5	COMPUTER GRAPHICS	




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CIRCULAR

Sub : Internal Assessment Test – I (Reg – 2021) EVEN SEM

- It is Informed that the Internal Assessment Test — I for FIRST YEAR UG Student will be scheduled from (26.6.2023 - 04.07.2023)

INTERNAL ASSESSMENT TEST - I SCHEDULE FOR I - YEAR (II - SEM)

SECTION	A	B	C	D
DATE / DEPT	AIDS, CIVIL	ECE,EEE	CSE,AI ML	IT,CS,MECH
26.6.2023	Professional English – II (HS3252)	Professional English – II (HS3252)	Professional English – II (HS3252)	Professional English – II (HS3252)
27.6.2023	Statistics and Numerical Methods (MA3251)	Statistics and Numerical Methods (MA3251)	Statistics and Numerical	Statistics and Numerical Methods
28.6.2023	Physics for Information Science (PH3256) - AIDS Physics for Civil Engineering (PH3201) - CIVIL	Physics for Electronics Engineering (PH3254) – ECE Physics for Electrical Engineering (PH3202) - EEE	Physics for Information Science (PH3256)	Physics for Information Science (PH3256) – IT,CS Materials Science (PH3251) - MECH
30.6.2023	Basic Electrical and Electronics Engineering (BE3251) – AIDS Basic Electrical and	Electrical and Instrumentation Engineering (BE3254) – ECE Basic Civil and Mechanical Engineering (BE3255) - EEE	Basic Electrical and Electronics Engineering (BE3251)	Basic Electrical and Electronics Engineering (BE3251)
01.7.2023	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)
03.7.2023	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)
04.07.2023	Data Structures Design (AD3251) - AIDS	Circuit Analysis (EC3251) - ECE	Programming in C (CS3251)	Programming in C (CS3251)



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CIRCULAR


All The HOD Are Hereby Informed To Complete MODEL EXAM For UG Students Between (1ST YEAR) And Also Submit 2 Set Of Question Paper To The Exam Cell On Or Before (29.7.2023) 12: 00. Allocation Of Marks For The Assessment Test Should Be As Prescribed Below.

Regulation – 2021

Part – A -----→ 7 X 2 = 14 (With Choice)
Part – B -----→ 2 X 13 = 26 (With Choice)
Part – C -----→ 1 X 10 = 10 (With Choice)
Total -----→ 50 Marks

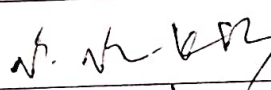
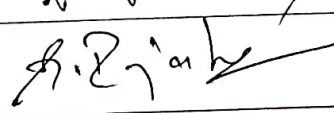
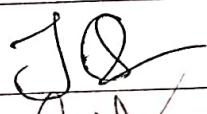
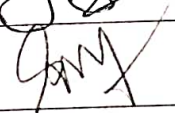

Exam Coordinator




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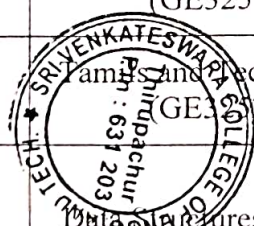
CIRCULAR

Sub : Internal Assessment Test – I (Reg – 2021) EVEN SEM

- It is Informed that the MODEL EXAM for FIRST YEAR UG Student will be scheduled from (01.08.2023 - 08.08.2023)

MODEL EXAM SCHEDULE FOR I-YEAR (II-SEM)

SECTION	A	B	C	D
DATE / DEPT	AIDS, CIVIL	ECE,EEE	CSE,AIML	IT,CS,MECH
01.08.2023	Professional English – II (HS3252)	Professional English – II (HS3252)	Professional English – II (HS3252)	Professional English – II (HS3252)
02.08.2023	Statistics and Numerical Methods (MA3251)	Statistics and Numerical Methods (MA3251)	Statistics and Numerical Methods (MA3251)	Statistics and Numerical Methods (MA3251)
03.08.2023	Physics for Information Science (PH3256) - AIDS Physics for Civil Engineering (PH3201) - CIVIL	Physics for Electronics Engineering (PH3254) – ECE Physics for Electrical Engineering (PH3202) - EEE	Physics for Information Science (PH3256)	Physics for Information Science (PH3256) – IT,CS Materials Science (PH3251) - MECH
04.08.2023	Basic Electrical and Electronics Engineering (BE3251) – AIDS Basic Electrical and Electronics Engineering (BE3251) – AIDS	Electrical and Instrumentation Engineering (BE3254) – ECE	Basic Electrical and Electronics Engineering (BE3251)	Basic Electrical and Electronics Engineering (BE3251)
05.08.2023	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)	Engineering Graphics (GE3251)
07.08.2023	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)	Tamils and Technology (GE3252)
08.08.2023	Data Structures Design (AD3251) - AIDS	Circuit Analysis (EE3251) - EEE	Engineering and Technology Programming in C (CS3251)	Programming in C (CS3251)



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All the HOD are hereby informed to complete the Internal Assessment Test – I for Second year UG students and also submit 2 set of question paper to the exam cell on or before **14.09.2022**, allocation of marks for the Internal Assessment Test should be as prescribed below.

Regulation – 2021

Part – A	----->	7 X 2 = 14	(With Choice)
Part – B	----->	2 X 13 = 26	(With Choice)
Part – C	----->	1 X 10 = 10	(With Choice)
Total	----->	50 Marks	

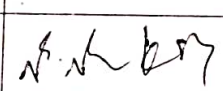
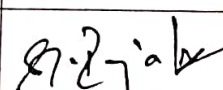
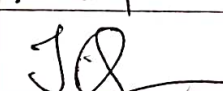
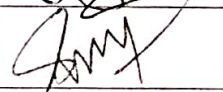
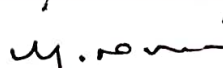

Exam Coordinator

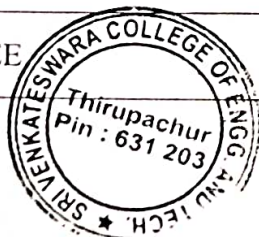




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Sub : Internal Assessment Test – I (Reg – 2021) ODD SEM

➤ It is Informed that the Internal Assessment Test — I for Second Year UG Student will be scheduled from (16/09/2022 – 21/09/2022)

INTERNAL ASSESSMENT TEST-I SCHEDULE FOR II-YEAR (III-SEM)

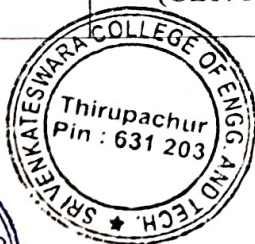
DATE	CIVIL	CSE	ECE	EEE	MECH
16/09/2022	Estimation, Costing and Valuation Engineering (CE8701)	Principles of Management (MG8591)	Antennas and Microwave Engineering (EC8701)	High Voltage Engineering (EE8701)	Power Plant Engineering (ME8792)
18/09/2022	Railways, Airports, Docks and harbors Engineering (CE8702)	Cryptography and Network Security (CS8792)	Optical Communication (EC8751)	Power System Operation and Control (EE8702)	Process Planning and Cost Estimation (ME8793)
19/09/2022	Structural Design and Drawing (CE8703)	Cloud Computing (CS8791)	Embedded and Real Time Systems (EC8791)	Renewable Energy Systems (EE8703)	Mechatronics (ME8791)
20/09/2022	Traffic Engineering and Management (CE8007)	Hospital Management (OBM752)	Ad hoc and Wireless Sensor Networks (EC8702)	Introduction to C Programming (OCS752)	Unconventional Machining Processes (ME8073)
21/09/2022	Creative and Innovative Project (Activity Based - Subject Related) (CE8711)	Multicore Architecture and Programming (CS8083)	Advanced Wireless Communication (EC8092)	Disaster Management (GE8071)	Non Destructive Testing and Evaluation (ME8097)

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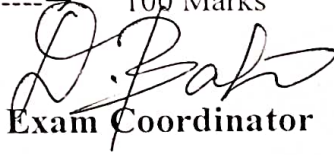
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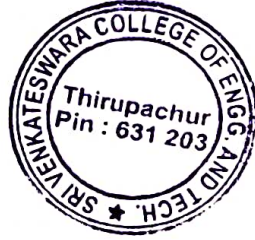
CIRCULAR

All the HOD are hereby informed to complete the Model Exam for Second year UG students and also submit 2 set of question paper to the exam cell on or before **16.09.2022**, allocation of marks for the Model Exam should be as prescribed below.

Regulation – 2021

Part – A -----→ 10 X 2 = 20 (With Choice)
Part – B -----→ 5 X 13 = 65 (With Choice)
Part – C -----→ 1 X 15 = 15 (With Choice)
Total -----→ 100 Marks

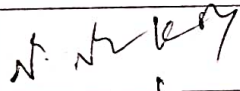
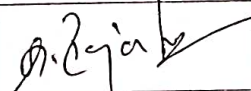
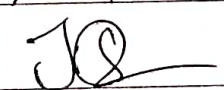
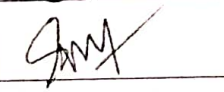
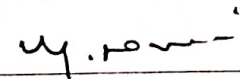

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Sub : Model Exam (Reg – 2021) ODD SEM

- It is informed that the Model Exam for 2nd year Student will be scheduled from (19/12/2022 – 24/12/2022)

MODEL EXAM SCHEDULE FOR II-YEAR (III-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
19.12.2022	Transforms and Partial Differential Equations (MA3351)	Discrete Mathematics (MA3354)	Random Processes and Linear Algebra (MA3355)	Probability and Complex Functions (MA3303)	Transforms and Partial Differential Equations (MA3351)
20.12.2022	Engineering Mechanics (ME3351)	Digital Principles and Computer Organization (CS3351)	Data Structures (CS3351)	Electromagnetic Fields (EE3301)	Engineering Mechanics (ME3351)
21.12.2022	Fluid Mechanics (CE3301)	Foundations of Data Science (CS3352)	Signals and Systems (EC3354)	Digital Logic Circuits (EE3302)	"Engineering Thermodynamics" (ME3391)
22.12.2022	Construction Materials and Technology (CE3302)	Data Structures (CS3301)	Electronic Devices and Circuits (EC3353)	Electron Devices and Circuits (EC3301)	Fluid Mechanics and Machinery (CE3391)
23.12.2022	Water Supply and Wastewater Engineering (CE3303)	Object Oriented Programming (CS3391)	Control Systems (EC3351)	Electrical Machines – I (EE3303)	Engineering Materials and Metallurgy (ME3392)
24.12.2022	Engineering and Level (CE3301)	Professional Development (GE3361)	Data Structures and OOPS (CS3352)	Manufacturing Processes (ME3393)	

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All the HOD are hereby informed to complete Assessment- 1 for 3rd and 4th year UG students and also submit 2 set of question paper to the exam cell on or before (26.08.2022), allocation of marks for the assessment test should be as prescribed below.

Regulation – 2021

Part – A	-----→	7 X 2 = 14 (With Choice)
Part – B	-----→	2 X 13 = 26 (With Choice)
Part – C	-----→	1 X 10 = 10 (With Choice)
Total	-----→	50 Marks


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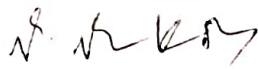
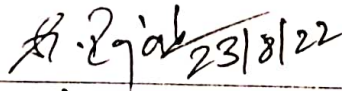

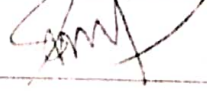
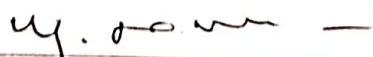

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Sub : Internal Assessment Test – I (Reg – 2017) ODD SEM

- It is informed that the Internal Assessment Test — I for 3rd year Student will be scheduled from (29/08/2022 – 02/09/2022)

INTERNAL ASSESSMENT TEST-I SCHEDULE FOR III-YEAR (V-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
29.08.2022	Design of Reinforced Concrete Structural Elements (CE8501)	Algebra and Number Theory (MA8551)	Digital Communication (EC8501)	Power System Analysis (EE8501)	Design of Machine Elements (ME8595)
30.08.2022	Structural Analysis I (CE8502)	Computer Networks (CS8591)	Discrete Time Signal Processing (EC8553)	Microprocessors and Microcontrollers (EE8551)	Metrology and Measurements (ME3592)
31.08.2022	Water Supply Engineering (EN8491)	Microprocessors and Microcontrollers (EC8691)	Computer Architecture and Organization (EC8552)	Power Electronics (EE8552)	Thermal Engineering - II (ME8595)
01.09.2022	Foundation Engineering (CE8591)	Theory of Computation (CS8501)	Communication Networks (EC8551)	Digital Signal Processing (EE8591)	Dynamics Of Machine (ME8594)
02.09.2022	Human Rights (GE807)	Object Oriented Analysis and Design (CS8592)	Medical Electronics (EC8073)	Object Oriented Programming (CS8392)	Internal Combustion Engine (OAT552)
03.09.2022	Environment (GE808)	Tele health Technology (OMD553)			



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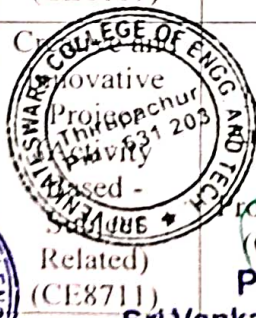
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Sub : Internal Assessment Test – I (Reg – 2017) ODD SEM

- It is informed that the Internal Assessment Test — I for 4th year Student will be scheduled from (29/08/2022 – 02/09/2022)

INTERNAL ASSESSMENT TEST-I SCHEDULE FOR IV-YEAR (VII-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
29.08.2022	Estimation, Costing and Valuation Engineering (CE8701)	Principles of Management (MG8591)	Antennas and Microwave Engineering (EC8701)	High Voltage Engineering (EE8701)	Power Plant Engineering (ME8792)
30.08.2022	Railways, Airports, Docks and harbors Engineering (CE8702)	Cryptography and Network Security (CS8792)	Optical Communication (EC8751)	Power System Operation and Control (EE8702)	Process Planning and Cost Estimation (ME8793)
31.08.2022	Structural Design and Drawing (CE8703)	Cloud Computing (CS8791)	Embedded and Real Time Systems (EC8791)	Renewable Energy Systems (EE8703)	Mechatronics (ME8791)
01.09.2022	Traffic Engineering and Management (CE8007)	Hospital Management (OBM752)	Ad hoc and Wireless Sensor Networks (EC8702)	Introduction to C Programming (OCS752)	Unconventional Machining Processes (ME8073)
02.09.2022	Innovative Project Based - Related (CE8711)	Multicore architecture and programming (CS8083)	Advanced Wireless Communication (EC8092)	Disaster Management (GE8071)	Non Destructive Testing and Evaluation (ME8097)



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All the HOD are hereby informed to complete internal assessment-II for 3rd and 4th year UG students and also submit 2 set of question paper to the exam cell on or before (30.09.2022), allocation of marks for the assessment test should be as prescribed below.

Regulation – 2017

Part – A	-----→	7 X 2 = 14 (With Choice)
Part – B	-----→	2 X 13 = 26 (With Choice)
Part – C	-----→	1 X 10 = 10 (With Choice)
Total	-----→	50 Marks

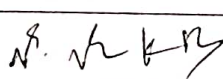
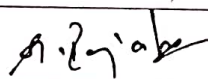
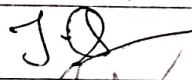
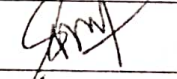
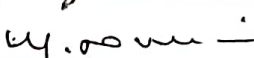

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Sub : Internal Assessment Test – II (Reg – 2017) ODD SEM

- It is informed that the Internal Assessment Test — II for 3rd year Student will be scheduled from (03/10/2022 – 08/10/2022)

INTERNAL ASSESSMENT TEST-II SCHEDULE FOR III-YEAR (V-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
03.10.2022	Design of Reinforced Concrete Structural Elements (CE8501)	Algebra and Number Theory (MA8551)	Digital Communication (EC8501)	Power System Analysis (EE8501)	Design of Machine Elements (ME8595)
04.10.2022	Structural Analysis I (CE8502)	Computer Networks (CS8591)	Discrete Time Signal Processing (EC8553)	Microprocessors and Microcontrollers (EE8551)	Metrology and Measurements (ME3592)
05.10.2022	Water Supply Engineering (EN8491)	Microprocessors and Microcontrollers (EC8691)	Computer Architecture and Organization (EC8552)	Power Electronics (EE8552)	Thermal Engineering - II (ME8595)
06.10.2022	Foundation Engineering (CE8591)	Theory of Computation (CS8501)	Communication Networks (EC8551)	Digital Signal Processing (EE8591)	Dynamics Of Machine (ME8594)
07.10.2022	Human Rights GE8074	Object Oriented Analysis and Design (CS8592)	Medical Electronics (EC8073)	Object Oriented Programming (CS8392)	Internal Combustion Engine (OAT552)
08.10.2022	Object Oriented and Agriculture (OAT552)	Tele health Technology (OMD553)		Sensors and Transducers (EE8551)	

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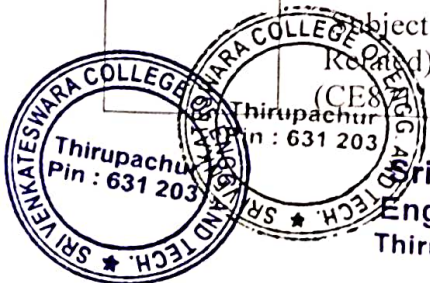
CIRCULAR

Sub : Internal Assessment Test – II (Reg – 2017) ODD SEM

- It is informed that the Internal Assessment Test — II for 4th year Student will be scheduled from (03/10/2022 – 07/10/2022)

INTERNAL ASSESSMENT TEST-II SCHEDULE FOR IV-YEAR (VII-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
03.10.2022	Estimation, Costing and Valuation Engineering (CE8701)	Principles of Management (MG8591)	Antennas and Microwave Engineering (EC8701)	High Voltage Engineering (EE8701)	Power Plant Engineering (ME8792)
04.10.2022	Railways, Airports, Docks and harbors Engineering (CE8702)	Cryptography and Network Security (CS8792)	Optical Communication (EC8751)	Power System Operation and Control (EE8702)	Process Planning and Cost Estimation (ME8793)
05.10.2022	Structural Design and Drawing (CE8703)	Cloud Computing (CS8791)	Embedded and Real Time Systems (EC8791)	Renewable Energy Systems (EE8703)	Mechatronics (ME8791)
06.10.2022	Traffic Engineering and Management (CE8007)	Hospital Management (OBM752)	Ad hoc and Wireless Sensor Networks (EC8702)	Introduction to C Programming (OCS752)	Unconventional Machining Processes (ME8073)
07.10.2022	Creative and Innovative Project (Activity Based - Subject (CE8008))	Multicore Architecture and Programming (CS8083)	Advanced Wireless Communication (EC8092)	Disaster Management (GE8071)	Non Destructive Testing and Evaluation (ME8097)



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Regulation – 2017

Part – A	-----→	10 X 2 = 20 (With Choice)
Part – B	-----→	5 X 13 = 65 (With Choice)
Part – C	-----→	1 X 15 = 15 (With Choice)
Total	-----→	50 Marks

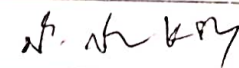
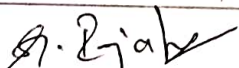


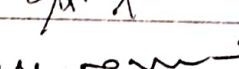

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5	EEE	




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Sub : Model Exam (Reg – 2017) ODD SEM

- It is Informed that the ,MODEL EXAM for Third year UG Student will be scheduled from (10/11/2022 - 16/11/2022)

MODEL EXAM SCHEDULE FOR III-YEAR (V-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
10.11.2022	Design of Reinforced Concrete Structural Elements (CE8501)	Algebra and Number Theory (MA8551)	Digital Communication (EC8501)	Power System Analysis (EE8501)	Design of Machine Elements (ME8595)
11.11.2022	Structural Analysis I (CE8502)	Computer Networks (CS8591)	Discrete Time Signal Processing (EC8553)	Microprocessors and Microcontrollers (EE8551)	Metrology and Measurements (ME3592)
12.11.2022	Water Supply Engineering (EN8491)	Microprocessors and Microcontrollers (EC8691)	Computer Architecture and Organization (EC8552)	Power Electronics (EE8552)	Thermal Engineering - II (ME8595)
14.11.2022	Foundation Engineering (CE8591)	Theory of Computation (CS8501)	Communication Networks (EC8551)	Digital Signal Processing (EE8591)	Dynamics Of Machine (ME8594)
15.11.2022	Human Rights GE8074	Object Oriented Analysis and Design (CS8592)	Medical Electronics (EC8073)	Object Oriented Programming (CS8392)	Internal Combustion Engine (OAT552)
16.11.2022	Environment and Agriculture	Telehealth Technology (OMD553)		Sensors and Transducers (OAN551)	-

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Sub : Model Exam (Reg – 2017) ODD SEM

- It is informed that the Model Exam for 4th year Student will be scheduled from (10/11/2022 – 15/11/2022)

MODEL EXAM SCHEDULE FOR IV-YEAR (VII-SEM)

DATE	CIVIL	CSE	ECE	EEE	MECH
10.11.2022	Estimation, Costing and Valuation Engineering (CE8701)	Principles of Management (MG8591)	Antennas and Microwave Engineering (EC8701)	High Voltage Engineering (EE8701)	Power Plant Engineering (ME8792)
11.11.2022	Railways, Airports, Docks and harbors Engineering (CE8702)	Cryptography and Network Security (CS8792)	Optical Communication (EC8751)	Power System Operation and Control (EE8702)	Process Planning and Cost Estimation (ME8793)
12.11.2022	Structural Design and Drawing (CE8703)	Cloud Computing (CS8791)	Embedded and Real Time Systems (EC8791)	Renewable Energy Systems (EE8703)	Mechatronics (ME8791)
14.11.2022	Traffic Engineering and Management (CE8007)	Hospital Management (OBM752)	Ad hoc and Wireless Sensor Networks (EC8702)	Introduction to C Programming (OCS752)	Unconventional Machining Processes (ME8073)
15.11.2022	Creative and Innovative Activity Based - Thirupachur Sub 631203 Related (CE8715)	Multicore Architecture and Programming (CS8083)	Advanced Wireless Communication (EC8092)	Disaster Management (EE8092)	Non Destructive Testing and Evaluation (ME8097)



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Regulation – 2021

Part – A -----→ 7 X 2 = 14 (With Choice)
Part – B -----→ 2 X 13 = 26 (With Choice)
Part – C -----→ 1 X 10 = 10 (With Choice)
Total -----→ 50 Marks

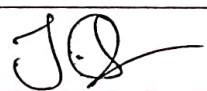
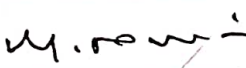
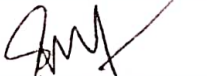

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3	ME - VLSI	




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Sub : Internal Assessment Test – I (Reg – 2021)

- It is informed that the Internal Assessment Test — I for Second Year PG Student will be scheduled from (26.06.2023 - 02.07.2023) .

INTERNAL ASSESSMENT TEST-I SCHEDULE FOR I-YEAR (II-SEM)

DATE	ME - CSE	ME – PED	ME - VLSI
26.06.2023	Internet of Things (CP4291)	Analysis of Electrical Drives (PX4201)	Design for Verification UVM (VL4251)
27.06.2023	Machine Learning (CP4252)	Special Electrical Machines (PX4202)	Low Power VLSI Design (VL4291)
28.06.2023	Multicore Architecture and Programming (CP4292)	Electric Technical and Power Management (PX4291)	RFIC Design (VL4292)
30.06.2023	Advanced Software Engineering (SE4151)	Power Electronic for Renewable Energy System (PX4005)	VLSI Testing (VL4252)
01.07.2023	Cloud Computing Technologies (MP4251)	Power Quality (PX4071)	ASIC Design (VL4071)
02.07.2023	Information Retrieval Techniques (CP4093)		System On Chip (I14092)



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Regulation – 2021


Part – A -----→ 7 X 2 = 14 (With Choice)
Part – B -----→ 2 X 13 = 26 (With Choice)
Part – C -----→ 1 X 10 = 10 (With Choice)
Total -----→ 50 Marks

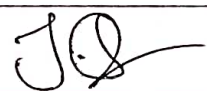
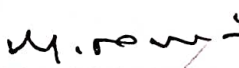
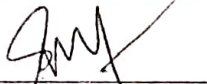

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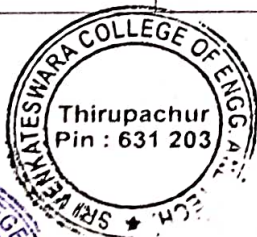
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Sub : Model Exam (Reg – 2021)

- It is Informed that the Model Exam for first Year PG
Student will be scheduled from (01.08.2023 - 07.08.2023)

MODEL EXAM SCHEDULE FOR I - YEAR (II-SEM)

DATE	ME - CSE	ME - PED	ME - VLSI
01.08.2023	Internet of Things (CP4291)	Analysis of Electrical Drives (PX4201)	Design for Verification UVM (VL4251)
02.08.2023	Machine Learning (CP4252)	Special Electrical Machines (PX4202)	Low Power VLSI Design (VL4291)
03.08.2023	Multicore Architecture and Programming (CP4292)	Electric Technical and Power Management (PX4291)	RFIC Design (VL4292)
04.08.2023	Advanced Software Engineering (SE4151)	Power Electronic for Renewable Energy System (PX4005)	VLSI Testing (VL4252)
05.08.2023	Cloud Computing Technologies (MP4251)	Power Quality (PX4071)	ASIC Design (VL4071)
07.08.2023	Information Retrieval Techniques (CP4093)	-	System On Chip (II4092)



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All the HOD are hereby informed to complete the assessment test – 1 for PG students (1st year) and also submit 2 set of question paper to the exam cell on or before (28.04.2023), allocation of marks for the Assessment Test should be as prescribed below.

Regulation – 2021

Part – A -----→ 7 X 2 = 14 (With Choice)
Part – B -----→ 2 X 13 = 26 (With Choice)
Part – C -----→ 1 X 10 = 10 (With Choice)
Total -----→ 50 Marks


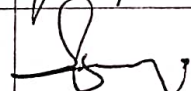

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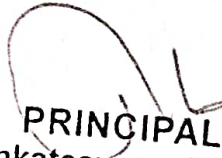

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2	MCA	




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Sub: Internal Assessment Test – I (Reg – 2021)

- It is informed that the Internal Assessment Test — I for MBA First Year PG Student will be scheduled from (04.05.2023 - 10.05.2023)

INTERNAL ASSESSMENT TEST-I SCHEDULE FOR 1-YEAR (MBA) (II-SEM)

DATE	SUBJECT
04.05.2023	Quantitative Techniques for Decision Making (BA4201)
05.05.2023	Financial Management (BA4202)
06.05.2023	Human resource Management (BA4203)
08.05.2023	Operations Management (BA4204)
09.05.2023	Business Research Methods (BA4205)
10.05.2023	Business Analytics (BA4206)



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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

SECOND YEAR - B.E/B.TECH - Regulation 2017

INTERNAL ASSESSMENT - I

CS3301 - DATA STRUCTURE

Mark : 50

Time : 10 : 30 – 12 : 30

Part A

- 1) Define Data Structure ?
- 2) Difference Between Linear and Non – Linear Data Structure ?
- 3) Comparison Between Array and Linked List
- 4) What is Stack ADT ?
- 5) Define Function Calls ?
- 6) List Out the Basic Operation of a Stack ?
- 7) Define Binary Search ?

Part B

- 8) Describe the following:
 - i. Applications of lists. (5)
 - ii. Polynomial manipulation. (8)
- (or)
- 9) List an algorithm to perform the following operations in a doubly linked list.
 - i. Insert a node at the end of the list. (6)
 - ii. Delete the last node in the list. (7)
- 10) Describe about stack ADT using array in detail. (13)
- (i) Give an algorithm for push and pop operations on stack using a linked list with an example.
- (ii) Describe the function to examine whether the stack is full () or empty ().


(or)

- 11) Describe Evaluating arithmetic expressions (13)

Part c

- 12) Describe Array-based implementation.
- (or)
- 13) Create an algorithm to add two polynomials using linked list. (15)




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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

SECOND YEAR - B.E/B.TECH – Regulation 2017

INTERNAL ASSESSMENT – 2

CS3301 - DATA STRUCTURE

Mark: 50

Time : 10 : 30 – 12 : 30

Part A

1. Deline a binary tree. Give an example. ?
2. Give the various types of rotations in AVL tree during the insertion of a node.?
3. Differentiate cyclic and acyclic graph. ?
4. What is hashing?
5. Select the best sorting method out of the following - insertion sort quick sort and merge sort and give justification.
6. Distinguish between linear and binary search technique.
7. Simulate the result of inserting 2, 1, 4, 5, 9, 3, 6, 7 into an initially empty AVL Tree. ?

Part B

8. Write an algorithm for preorder, inorder and postorder traversal of a binary tree.

(or)

9. Explain the following operations on a binary search tree with suitable algorithm
 - i) Find a node
 - ii) Find minimum and maximum
10. State Kruskal's algorithm

(or)

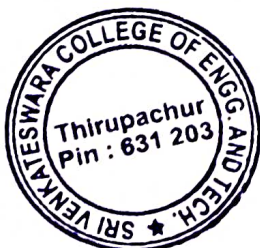
11. Examine the algorithm for Insertion sort and sort the following array:39,9,45,63,18,81, 108,54,72,36

Part C

12. State Euler circuits.

(or)

13. Interpret an algorithm to sort a set of 'N' numbers using bubble sort and demonstrate the sorting steps for the following set of numbers:
30, 52, 29, 87, 63, 27, 19, 54.




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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

SECOND YEAR - B.E/B.TECH - Regulation 2017

INTERNAL ASSESSMENT - I

CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

Mark : 50

Time : 10 : 30 – 12 : 30

Part A

1. What is a priority encoder?
2. Define Combinational circuit?
3. Define Karnaugh map ?
4. What are the Limitation of K – Map ?
5. Draw the circuit for 2 to 1 multiplexer circuit. and Give functional b
2 * 1 MUX ?
6. What is flip-flop?
7. When is a counter said to suffer from lockout?

Part B

8. i. Design a 4 bit adder / subtractor circuit and explain.
ii. What is BCD adder? Design an adder to Perform Arithmetic Addition of Two decimal
digits in BCD.

(or)

9. Explain in detail about Encoders and Decoders.
10. Design a MOD-10 Synchronous counter using JK flip – flop , Write Excute Table and state table.

(or)

11. Design a logic circuit diagram for 3-bit synchronous up-down counter.

Part C


12. Simplify the following Boolean into (i) SOP form and (ii) POS form and Implement the Simplified Function using AND ,
OR Gates ?

$$F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$$

(or)

13. A sequential circuit with two 'D' Flip – flop A and B one input (x) and one output (y)
The Flip-Flop input functions are: $DA = Ax + Bx$ $DB = A'x$ and the Circuit output function
is, $Y = (A + B)x'$.




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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

SECOND YEAR - B.E/B.TECH – Regulation 2017

INTERNAL ASSESSMENT – 2

CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

Mark : 50

Time : 10 : 30 – 12 : 30

Part A

1. What is Meant by Operands ?
2. Difference between memory location and memory address.?
3. What are the Types of Addressing Modes ?
4. Define data hazard. ?
5. Define Pipelining ?
6. Define Cache Memory ?
7. Define SATA ?

Part B

8. What are the Addressing Modes ? Explain the Various Addressing Modes with Examples ?
(or)
9. With Neat Diagram , Describe about Von Neuman Architecture ?
10. Write a short note on Data hazard and Control Hazards ?
(or)
11. Describe the data path and control considerations for pipelining.

Part B

12. Explain DMA Controller With the Block Diagram ?
(or)
13. Explain the various Mapping Techniques Associated With the Cache Memory ?




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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

SECOND YEAR - B.E/B.TECH – Regulation 2017

MODEL EXAMINATION

CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

Mark : 100

Time : 12 : 30 – 3: 30


Part A

1. List various logical operations supported by MIPS ?
2. Compare Machine Level , Assembly Level, and Higher Level Language ?
3. Why is Multiplexer ?
4. Define a latch and a flip flop ?
5. What are data transfer instructions ?
6. Outline instruction cycle with a diagram ?
7. What is a Program Counter ?
8. Define Pipelining ?
9. What is Hit Time ?
10. What is a Direct – Mapped cache ?

Part B (5 x13 = 55)

11. (a) (i) How will you design a Full adder using two half adders (7)
(ii) Simplify the Function using Multiplexer $f = \sum (0,1,3,4,8,9,15)$ (6)
(Or)
(b) (i) Demonstrate 4 bit magnitude comparison with three Outputs
 $A > B$, $A = B$, $A < B$
(ii) Build a 4 bit Priority encoder using gates ?
12. (a) (i) Realise D flip flop using SR flip flop
(ii) Construct a 4 bit down counter using logic gates
(Or)
(b) Give the analysis and design of clocked sequential circuits .
13. (a) (i) Explain the functional units in digital computer
(ii) Discuss about instruction cycle




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(Or)

- (b) (i) Explain about encoding in assembly language and types of instructions
(ii) Discuss the Interaction between assembly language and high level language.
14. (a) An instruction pipelined has five stages where each stage takes 2 nanoseconds and all instruction use all five stages, branch instruction are not overlapped (i.e) the instruction after the branch is not fetched till the branch instruction is completed. Under ideal condition .
Calculate the average instruction execution time assuming that 20% of all instruction executed are branch instruction. Ignore the fact that some branch instruction may be conditional.

(Or)

- (b) (i) What is Hazard ? Give hazard free realization for the following Boolean function
 $F(A,B,C,D) = \sum m(1,5,6,7)$ using AND – OR gates networks ? (10)
(ii) Defined essential hazards (3)
15. (a) (i) Explain in detail about DMA operation
(ii) Give the modes of DMA transfer

(Or)

- (b) Elucidate interconnection standards.

Part B

(1 x15= 15)

16. (a) Explain the functions with the state diagram and characteristic equation of T ,D and JK flip flop. Compare and contrast
(Or)
- (b) Implement the following Boolean function using 8 x 1 multiplexer.
Considering D as the input and A,B ,C as selection lines
 $F(A,B,C,D) = AB' + BD + B'CD'$.



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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

SEATING ARRANGEMENT FOR CSE


ASSESSMENT TEST - I

CLASS ROOM : F301

S. No	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
1	112422104001	112421104003	112420104007	112422104007
2	112421104001	112420104005	112421104005	112420104009
3	112420104002	112422104003	112422104005	112421104007
4	112422104002	112421104004	112420104008	112422104008
5	112421104002	112420104006	112421104006	112420104010
6	112420104003	112422104004	112422104006	112421104008

S. No	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
1	112422104010	112421104013	112420104016	112422104017
2	112421104010	112420104014	112421104017	112420104018
3	112420104011	112422104012	112422104015	112421104019
4	112422104011	112421104015	112420104017	112422104018
5	112421104012	112420104015	112421104018	112420104019
6	112420104012	112422104013	112422104016	112421104020




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S. No	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
1	112422104019	112421104023	112420104024	112422104025
2	112421104021	112420104022	112421104026	112420104026
3	112420104020	112422104021	112422104023	112421104028
4	112422104020	112421104025	112420104025	112422104026
5	112421104022	112420104023	112421104027	112420104027
6	112420104021	112422104022	112422104024	112421104029

S. No	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
1	112422104027	112421104034	112420104308	112422104303
2	112421104030	112420104305	112421104036	112420104310
3	112420104302	112422104029	112422104301	112421104038
4	112422104028	112421104035	112420104309	112422104304
5	112421104033	112420104306	112421104037	112420104311
6	112420104304	112422104030	112422104302	112421104039




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Date: 02.11.2022

REVISED - I**CENTRE FOR ACADEMIC COURSES**

ANNA UNIVERSITY : CHENNAI - 600 025

ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES**August 2022 – December 2022 (Semester III)**

UG (FT/PT) & PG (FT/PT) Degree Programmes

Sl. No.	Programme	Semester	Commencement of Classes	Last working day		Commencement of Practical Examinations		Commencement of End Semester Examinations	
				Existing	Revised	Existing	Revised	Existing	Revised
1	B E / B.Tech (Full-Time)	III	22.08.2022	08.12.2022	27.12.2022	10.12.2022	18.01.2023	21.12.2022	29.12.2022
2	B Arch (Full-Time)	III	22.08.2022	08.12.2022	-	10.12.2022	18.01.2023	21.12.2022	29.12.2022
3	B E / B.Tech (Part-Time)	III							
4	M B A (5 Yrs-Integrated)	III							
5	M B A (Full-Time & Part-Time)	III	01.09.2022	19.12.2022	-	21.12.2022	18.01.2023	02.01.2023	29.12.2022

RE - OPENING DAY FOR THE NEXT SEMESTER: 01.02.2023 (Wednesday)**NOTE:**

1. The Theory and Practical Examination schedules will be published in due course (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.



DAC -

02/11/2022
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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

AUGUST 2022 – DECEMBER 2022 - (SEMESTER - III)

UG (B.ARCH) Degree Programmes

Report No	Report Period	Test Period	Report Entry Period
I	22-08-2022 – 26-09-2022	20-09-2022 – 26-09-2022	29-09-2022 – 06-10-2022
II	27-09-2022 -- 03-11-2022	25-10-2022 -- 03-11-2022	03-11-2022 -- 09-11-2022
III	04-11-2022 – 08-12-2022	02-12-2022 – 08-12-2022	08-12-2022 –10-12-2022

Saturdays may be included as working days to make good the Shortages, if any.



P. Sankarvel
19.09.2022
CONTROLLER OF EXAMINATIONS

As
19-09-22

[Signature]
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Internal Assessment Schedule for Non Autonomous Affiliated Institutions

SEPTEMBER 2022 – DECEMBER 2022 - (SEMESTER - III)

PG (FT&PT) Degree Programmes - M.B.A.

Report No	Report Period	Test Period	Report Entry Period
I	01-09-2022 – 26-10-2022	19-10-2022 – 26-10-2022	26-10-2022 – 01-11-2022
II	27-10-2022 -- 19-12-2022	13-12-2022 -- 19-12-2022	19-12-2022 -- 21-12-2022

Saturdays may be included as working days to make good the Shortages, if any.

P. Sankaranarayanan
19.09.2022
CONTROLLER OF EXAMINATIONS



[Signature]
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ANNA UNIVERSITY:: CHENNAI 600 025

Internal Assessment Schedule for Non Autonomous Affiliated Institutions

OCTOBER 2022 – FEBRUARY 2023 - (SEMESTER – III)

PG (FT) Degree Programmes - M.C.A.

Report No	Report Period	Test Period	Report Entry Period
I	19-10-2022 – 10-12-2022	05-12-2022 – 10-12-2022	19-12-2022 – 23-12-2022
II	12-12-2022 -- 04-02-2023	30-01-2023 -- 04-02-2023	04-02-2023 -- 06-02-2023

Saturdays may be included as working days to make good the Shortages, if any.



16/12/2022

16.12.2022

P. Sankaranarayanan
16.12.2022

CONTROLLER OF EXAMINATIONS

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Thirupachur, Tamil Nadu - 631 203

Date: 06.10.2022

CENTRE FOR ACADEMIC COURSES
ANNA UNIVERSITY: : CHENNAI – 600 025
ACADEMIC SCHEDULE FOR NON-AUTONOMOUS AFFILIATED COLLEGES
October 2022 – February 2023 (SEMESTER I)
PG (FT/PT) Degree Programmes



Sl. No	Programme	Semester	Commencement of Classes	Last working day	Commencement of Practical Examinations	Commencement of End Semester Examinations
1.	M.B.A. (Full-Time & Part-Time)	I	10.10.2022	25.01.2023	27.01.2023	06.02.2023
2.	M.B.A. (5 Yrs-Integrated)					

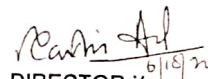
RE-OPENING DAY FOR THE NEXT SEMESTER: 08.03.2023 (Wednesday)

NOTE:

1. The Theory and Practical Examination schedules will be published in due course. (Practical Examinations will be conducted before the theory examinations).
2. If necessary, loss of classes due to various curricular / co-curricular activities of the department / college may be compensated by conducting classes on Saturdays.



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DIRECTOR i/c
ACADEMIC COURSES

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2. ALLOTMENT OF A PROJECT

- The student should spend a lot of time working with their project, so it is essential to pick a project they choose.
- Student chose a particular project doesn't mean that they are qualified to do it.
- Project Coordinator and supervisor should ensure that whether they are capable of doing that project in successful manner.
- Students are encouraged to choose more inter disciplinary and industrial projects.

FORMATION OF A PROJECT GROUPS

- In order to ensure the participation of each student, The Project size shall be restricted to 3
- Formation of project groups shall be done such that each group has representation of students with varying academic merit from best to average as well as mix domain expertise.
- Any left out student should be randomly attached to any group.

PROJECT WORK ASSESSMENT PLAN			
Internal Assessment (50%)	Zeroth Review		10
	Review – 1		30
	Review – 2		30
	Review – 3		30
	Overall Internal Marks		100 Marks
External Assessment (50%)	Report Evaluation	Internal Examiner	20
		External Examiner	30
	Viva Voce	Internal Examiner	20
		External Examiner	30
	Overall External Marks		100 Marks

GENERAL RULES AND REGULATION

- In House Project Students Must Meet Their Guide Every Day To Discuss About The Project Developments And Attendance Record Has To Be Duly Signed By Their Guide.
- The Supervisor Should Cultivate and Inculcate the Knowledge On Inter Disciplinary Project.
- It Is Mandatory For The Student To Contact Their Respective Guide And Discussion Has To Be Recorded In Their Project



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9	(112420104014) (112420104327) (112420104311)	LOGESHWARAN G RAMKUMAR L INDHUMATHI S	AC REPAIRING SYSTEM	SANGEETHA.J
10	(112420104308) (112420104332) (112420104007)	GOPINATH M SANGAVI M DINESH P	EMERGENCY AMBULANCE HIRING PORTAL	JAYASRI J
11	(112420104026) (112420104008) (112420104010)	STEPHEN R DIVIN KUMAR M INBATAMIZHAN A	SECURITY GUARD HIRING SYSTEM	SANGEETHA.J
12	(112420104331) (112420104330) (112420104336)	SABEESH KUMAR S RISHIKUMAR R THAMIZHENDRAL R	SIGN TONE DEAF COMPANION SYSTEM TWO-WAY COMMUNICATION BETWEEN DEAF AND NON- DEAF INDIVIDUALS	SANGEETHA.J
13	(112420104319) (112420104309) (112420104326)	MUGESH KUMAR HARIKRISHNAN.R PREM KUMAR S	PPT GENERATOR	SANGEETHA.J

UG STUDENT PROJECT GUIDELINES

1. IMPORTANCE OF UG PROJECTS, GUIDELINES AND PROJECT COORDINATOR

- The final year project is the most important aspect during the course of our Engineering degree.
- Engineering is application of Knowledge. The application must be carried out with Judgment, to ensure that the resultant system is efficient and beneficial projects will be used as a discriminator to decide the quality of an engineering student.
- The Guideline are given for successful completion of BE / B Tech projects by facilitating uniform regulation in carrying out the projects.
- The Department will designate faculty member as the project coordinator
- The project coordinator has to make certain that project related activities, such as conducting reviews and keeping records are done regularly.
- The importance issues to be addressed while pursuing the projects are

1. Selection of a Project
2. Planning, Executing and managing a project
3. Documenting a Project
4. Assessment of a project




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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING BE - PROJECT WORK BATCH 2020 – 2024

BATCH NUM	REGISTER NUM	STUDENT NAME	PROJECT TITTELE	GUIDE NAME
1	(112420104015) (112420104002) (112420104016) (112420104314)	MANESH P ANBU J PERUMAL V KANIMOZHI P	EFFORT TRACKING SYSTEM	ANBARASI M K
2	(112420104012) (112420104006) (112420104027)	KATHIRAVAN M DEEPAK KUMAR V TAMILARASAN G	COLLEGE ENQUIRY CHATBOX	JAYASRI J
3	(112420104018) (112420104025) (112420104003)	POOJA V SHABANA S ANITHA V	BLOOD BANK AND DONOR MANAGEMENT SYSTEM	SANGEETHA.S
4	(112420104009) (112420104020) (112420104011)	DIVYA S RENUKA S KALAIVANI G	SMART IRRIGATION USING IDENTIFYING PLANT DISEASE AND WEATHER CONDITION	ANBARASI M K
5	(112420104315) (112420104023) (112420104017)	KEERTHANA S SARANYA R POOJA S	CRIMINOLOGICAL FINGERPRINT MATCHING ON PARTIAL PRINTS WITH HOUGH TRANSFORMED MINUTIAE DESCRIPTORS.	PADMAPRIYA K
6	(112420104019) (112420104024) (112420104022)	RAMYA R SARASWATHI M SANTHA KUMARI D	VARIOUS DISEASE PREDICTIONS USING CONVOLUTIONAL NEURAL NETWORKS	SANGEETHA.S
7	(112420104305) (112420104310) (112420104304)	ANU P HEMA T AKCIYA A	ANCIENT TAMIL CHARACTER RECOGNITION AND SPEECHABLE AUDIO FROM STONE INSCRIPTION	PADMAPRIYA K
8	(112420104332) (112420104005)	SANJIV S BALAJI GANESH S	A DEEP LEARNING BASED DEAF COMPANION SYSTEM FOR TWO WAY COMMUNICATION BETWEEN DEAF AND NON – DEAF INDIVIDUALS	SANGEETHA.J



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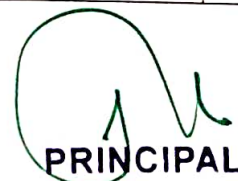
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✓ Vote Of Thanks Was Given By J.Sangeetha Imtiaz N And All The Parents Departed By 03.15 Pm

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
ME - PROJECT WORK BATCH 2021 – 2023

S.NO	REGISTER NUM	STUDENT NAME	PROJECT TITTELE	GUIDE NAME
1	12421405001	ANBARASI MK	SECURE FILE STORAGE ON CLOUD USING HYBIRD CRYPTOGRAPHY	MRS . DIVYA M. / AP
2	112421405002	BABY SHALINI G	DEMONSTRATION OF ROBOTIC VIRTUAL KEYBOARD ACCESSING	MS . SANGEETHA . J / AP
3	112421405003	BHARATHWAJ . V	HEALTH CARE RECOMMENDATION SYSTEM USING MACHINE LEARNING TECHNIQUES	MS . SANGEETHA . J / AP
4	112421405004	BRINDHA TV	AN AUTOMATED SYSTEM FOR ACCURATE SKIN DISESE DIAGNOSIS USING CNN WITH ADAM OPTIMIZER ALOGORITHM	MRS . SUREKHA RAJ .R / AP
5	112421405005	DEEPAK RAJ R	DATA FRAME WORK FOR SMALL SCALE PROVINCIAL FARMERS	MS . SANGEETHA . J / AP
6	112421405006	FANCY K	A HYBRID CLOUD APPROACH FOR SECURE AUTHORIZED DEDUPLICATION SYSTEM USING FACIAL AUTHENTICATION	MRS . DIVYA M. / AP
7	112421405009	JAYA SRI. J	KIDNEY STONE DETECTION BY USING NEURAL NETWORK CLASSIFIER	MS . SANGEETHA . J / AP
8	112421405013	PRAVEEN DEVA KUMAR MR	SMART FARMING VOICE SITE PLATFORM BY PHONE	MS . SANGEETHA . J / AP
9	112421405015	SHILPA S	WEATHER IMAGE CLASSIFICATION USING CONVOLUTION NEURAL NETWORK	MS . SWETHA M / AP
10	112421405016	VIJAYASREE M	COVID – 19 & PNEUMONIA CLASSDIFICATION USING DEEP LEARNING TECHNIQUE	MRS DIVYA S / AP




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CS3251 - PROGRAMMING
IN C

Reg. No : 112123104001

PART - B

43
50
[Signature]

11

(a) Looping Statements :

⇒ Repeat the program again and again until the condition is met is known

as iteration or looping

⇒ looping statements are also known as

Iterative statements.

⇒ It evaluates the coding constant and evaluates until the condition comes true



of looping

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⇒

- (i) For statement .
- (ii) While statement .
- (iii) Do-while statement .

(9) FOR STATEMENT :

⇒ For statement check the condition until whether it is true .

⇒ For statements are classified into three sections :

- (1) Initialization Section .
- (2) Condition Section .
- (3) Manipulation Section / Increment (or) decrement section .

(1) Initialization Section :

It Initialize the Value .

eg: $i = 1$.

(2)



Condition Section /

It checks whether the condition

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is satisfied and hence checks the true or false.

Eg: $(9 < 10)$

(3) Increasing / decreasing section :

After the condition check, the increasing / decreasing section will execute.

Eg: $(++i)$

Syntax for FOR LOOP :-

```
for ( Initialization ; Condition Test ; Increasing  
      decreasing section )  
{  
    Statement (s) ;  
}
```



In for loop not contains semicolon

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```
# include <stdio.h>
```

```
void main ()
```

```
{
```

```
for (i = 1, i <= 6, ++i)
```

```
{
```

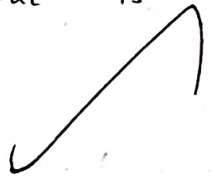
```
printf ("The output is : i")
```

```
scanf ("%d\n", i)
```

```
}
```

Output :

The output is

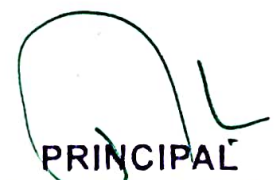


1
2
3
4
5
6

(11)



Loop :



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while loop also executes the

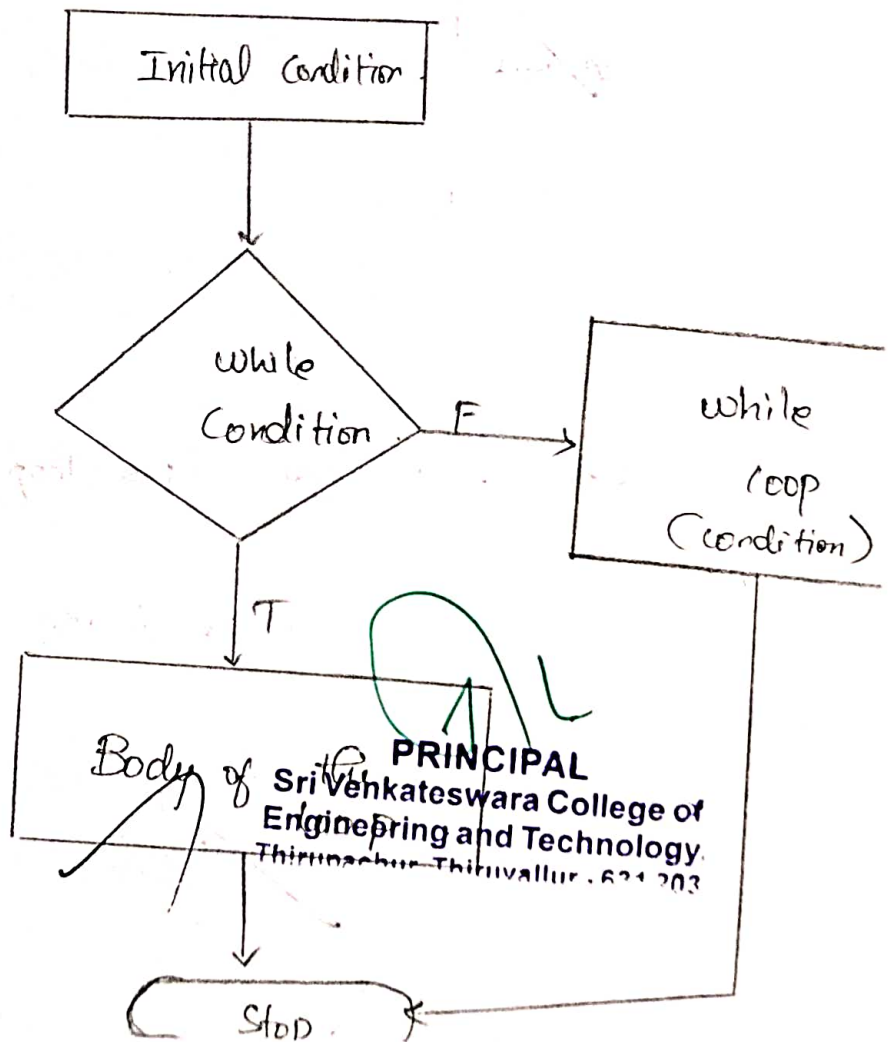
condition repeatedly until the condition

is met .

Syntax :

```
while (condition)
{
    statements;
}
```

Flow chart :



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Program to execute while loop :

```
#include <stdio.h>
```

```
void main ()
```

```
{  
  while (i = 1, i < 04)
```

```
{
```

```
    scanf ("%d/n", &i);
```

```
}
```

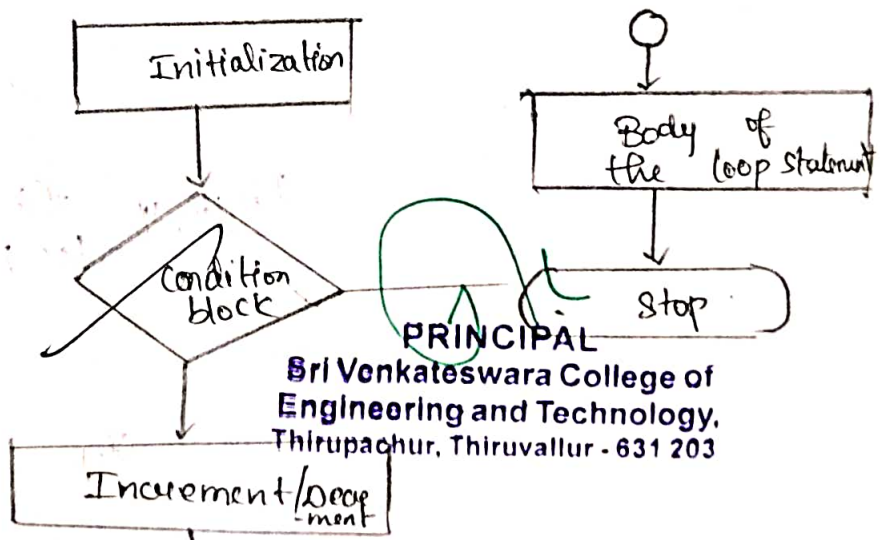
```
    printf (" i = %d\n", i);
```

```
}
```

Output :

```
i = 1,  
2  
3
```

Flow Chart for (For loop) :



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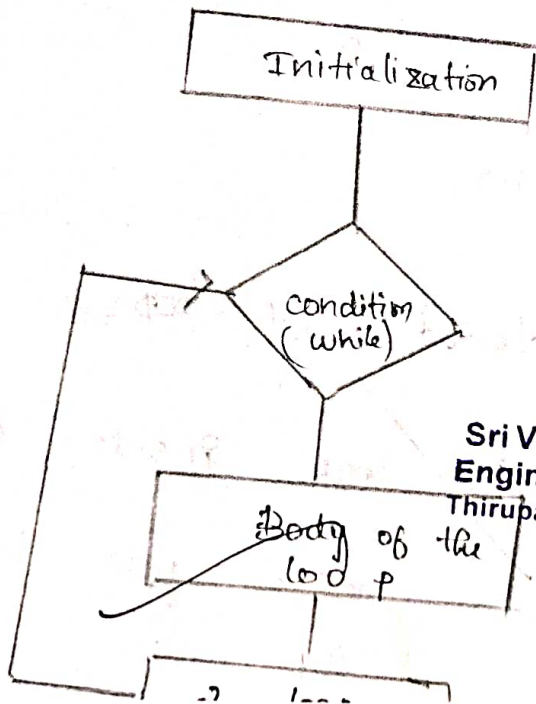
Loop :

⇒ Do while loop executes from the bottom.

⇒ Do while loop has the semicolon for the while condition statements.
Syntax for Do while loop:

```
do  
{  
while (Condition);  
}
```

Flow chart :



(Bottom approach)

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```
# include <stdio.h>
```

```
void main ( )
```

```
do
```

```
{
```

```
while (i >= 0 ; i <= 9);
```

```
{
```

```
scanf ( " %d \n " ; &i );
```

```
}
```

```
}
```

Output :

i = 0,

1,

2,


3.



loops :

Nested loop :

⇒ A for loop inside another for loop
is called nested for loop


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Syntax for Nested for loop:

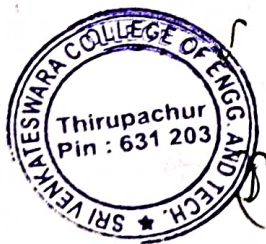
```
for  
{  
    Statement (s);  
    {  
        for  
        {  
            Statement (s);  
        }  
    }  
}
```

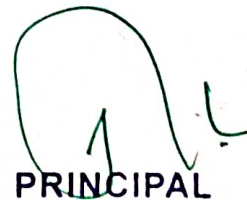
(ii) Nested while loop:

⇒ A while loop inside another while loop is called nested while loop.

Syntax:

```
while  
{  
    Statement (s);  
    while  
    {  
        Statement (s);  
    }  
}
```




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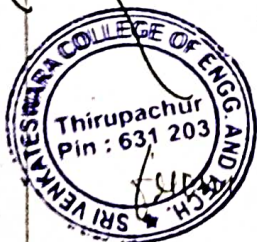
(iii) Nested do-while loop:

A loop inside another do while loop is called nested do-while loop.

Syntax:

```
do
{
    while (condition);
}
do
{
    while (condition2);
}
}
```

Also, in C programming apart



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break statements, looping, Switch statements,

Continue statements also available.

(10)

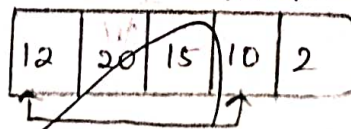
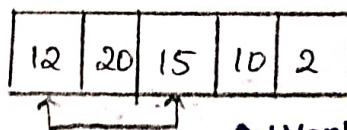
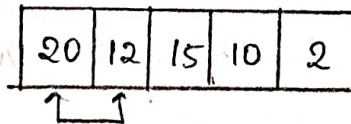
(b) Selection Sort :

⇒ finding the increasing or decreasing order of the number linearly in a given data is known as the Selection Sorting.

⇒ Selection is a method to find the numbers here, we choose the increasing (or) ascending order manner.

For Example :

Step 1 :



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2	10	12	20	15
---	----	----	----	----

Step 2:

2	10	12	20	15
---	----	----	----	----

↔

2	10	12	20	15
---	----	----	----	----

↔

2	10	12	20	15
---	----	----	----	----

↔

2	10	12	20	15
---	----	----	----	----

Step 3:

2	10	12	20	15
---	----	----	----	----

↔

2	10	12	15	20
---	----	----	----	----



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In Selection

Self, check the

Condition whether the number is
than that before number, it is

A number

C Program on Selection Sort :

```
#include <stdio.h>
```

```
void main ()
```

```
{
    int (i, j, n, temp);
```

```
{
```

```
    printf ("Enter the Number of array:");
```

```
    scanf ("%d", &n);
```

```
{
```

```
    printf ("Enter the array elements : ");
```

```
    scanf ("%d", &a[i]);
```

```
}
}
```

```
for (i=1, i < n, ++i)
```

```
    for (j=i+1, j < n, ++j)
```

```
        scanf ("%d", &a[j]);
```

```
    for (i=1, i < n, ++i)
```

```
    }
```

```
    temp = a[i];
```



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Print f (" Sorted list : ");

scanf ("%d", & n);

}

Out put :

Enter the Number of array : 5

Enter the Array elements :

8	2	9	19	6
---	---	---	----	---

The Sorted List :

2	6	8	9	19
---	---	---	---	----



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PART - C :

(13)

(6) Structure of C.

Documentation Section

Linked section

Definition Section

Global Declaration Section

Main function ()

Declaration part

Executable part

Subprogramming section

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Function 1

Function 2

user defined function



(i) Documentation Section :

⇒ Documentation Section is the Initialization of the C-program.
⇒ Documentation Section also includes the Comment line statements.

(ii) Linked Section :

⇒ Linked Section includes the Preprocessor directives such as #include

in the user defined functions.

⇒ Example for linked section is .

#include



Definition

section

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⇒ Definition section has the

directives of # define module as
the function.

(iv) Global declaration section :

⇒ It contains the user getting
or an Input function values.

⇒ we have to declare the variables
and the elements in the global
declaration section.

(v) Main Function () :

⇒ Main function () in the C program
has classified into two types :

Declaration part :

we have to declare the variable in
the declaration part before the execution of



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- Executable part will open with the open braces and closed with the closed braces.
- definitely the braces are must for the main function () section in the program.
- ⇒ The closed braces are the end of the part and it move on to the function body.

(vi) Sub programming section :

→ Sub programming section is the user defined function section.

which includes the function and in linear manner the user defined function.



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example program in structure of C :

```
#include <stdio.h>
#include <conio.h>
```

```
void main ()
```

```
{
  # user defined functions
```

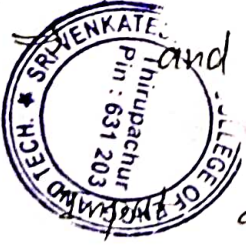
```
for ( i=1, i<3, ++i )
```

```
printf ( " The increment value is : " );
scanf ( " %d/n " ; & i );
```

PART - A

1) use of main () function :

→ main () function in a C-program would give about the user defined functions.



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2)

→ The input statements and output statements in C :

⇒ The output statements in C-program is printf.

3) Preprocessor:

⇒ Preprocessor is a already created user defined module in C-program.

⇒ which is processed early and which is # include.

4) Preprocessor directive:

⇒ Preprocessor directives is # include.

7) String:

⇒ String is a collection of elements which is enclosed with a single or double quote.



⇒ String can perform many operations.

known as string concatenation, str(len).

str(cmp).

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TIME TABLE FOR M.E./M.TECH./M.ARCH DEGREE EXAMINATIONS- NOV./DEC.-2022
Regulations : 2021

Page : 7 of 29


Branch:M.E. Computer Science and Engineering


II Semester	Session :	2.00 P.M. to 5.00 P.M.
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	CP4097:Web Analytics
05/04/2023	Wednesday	BD4071:High Performance Computing for Big Data
05/04/2023	Wednesday	BD4251:Big Data Mining and Analytics
06/04/2023	Thursday	CP4093:Information Retrieval Techniques
10/04/2023	Monday	CP4291:Internet of Things
11/04/2023	Tuesday	SE4151:Advanced Software Engineering
12/04/2023	Wednesday	CP4292:Multicore Architecture and Programming
18/04/2023	Tuesday	CP4252:Machine Learning

Branch:M.E. Energy Engineering

II Semester	Session :	10.00 A.M. to 01.00 P.M.
Exam Date	Day	Sub.Code/Name
06/04/2023	Thursday	EY4202:Computational Fluid Dynamics for Energy Systems
12/04/2023	Wednesday	EY4201:Energy Conservation in Industrial Utilities
17/04/2023	Monday	EY4203:Energy Efficient Buildings Design
18/04/2023	Tuesday	EY4071:Bio Energy Technologies
19/04/2023	Wednesday	EY4008:Solar Energy Technologies
19/04/2023	Wednesday	EY4002:Power Generation Transmission and Distribution
III Semester	Session :	10.00 A.M. to 01.00 P.M.
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	CX4016:Environmental Sustainability
10/04/2023	Monday	EY4091:Advanced Energy Storage Technologies
10/04/2023	Monday	TE4092:Design of Heat Exchangers
11/04/2023	Tuesday	TE4091:Advanced Power Plant Engineering
11/04/2023	Tuesday	EY4005:Wind Energy systems
11/04/2023	Tuesday	EY4004:Power Electronics for Renewable Energy Systems
13/04/2023	Thursday	EY4007:Environmental Engineering and Pollution Control
21/04/2023	Friday	PX4012:Renewable Energy Technology




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TIME TABLE FOR M.C.A. DEGREE EXAMINATIONS - NOV./DEC. - 2022
(Regulations : 2021)
CHOICE BASED CREDIT SYSTEM (CBCS)

Branch: Master of Computer Applications (2 Years)

I Semester		
Exam Date	Day	Sub.Code/Name
13/02/2023	Monday	MA4151: Applied Probability and Statistics for Computer Science Engineers
15/02/2023	Wednesday	MC4101: Advanced Data Structures and Algorithms
17/02/2023	Friday	RM4151: Research Methodology and IPR
21/02/2023	Tuesday	MC4102: Object Oriented Software Engineering
23/02/2023	Thursday	MC4103: Python Programming
25/02/2023	Saturday	MC4104: Fundamentals of Accounting
27/02/2023	Monday	BX4001: Data Structures and Algorithms
01/03/2023	Wednesday	BX4002: Problem Solving and Programming in C
II Semester		
Exam Date	Day	Sub.Code/Name
13/02/2023	Monday	MC4201: Full Stack Web Development
15/02/2023	Wednesday	MC4202: Advanced Database Technology
17/02/2023	Friday	MC4203: Cloud Computing Technologies
21/02/2023	Tuesday	MC4204: Mobile Application Development
23/02/2023	Thursday	MC4205: Cyber Security
25/02/2023	Saturday	MC4007: Operations Research
25/02/2023	Saturday	MC4006: Soft Computing Techniques
25/02/2023	Saturday	MC4005: Information Retrieval Techniques
25/02/2023	Saturday	MC4004: Advances in Operating System
25/02/2023	Saturday	MC4003: E - Learning
25/02/2023	Saturday	MC4002: Professional Ethics in IT
25/02/2023	Saturday	MC4001: Software Project Management
25/02/2023	Saturday	MC4008: Business Data Analytics
27/02/2023	Monday	BX4003: Introduction to Computer Organization and Operating Systems
01/03/2023	Wednesday	BX4004: Database Management Systems




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Regulations : 2021

Branch: M.E. Power Electronics and Drives

II Semester	Session :	10.00 A.M. to 01.00 P.M.
Exam Date	Day	Sub.Code/Name
10/04/2023	Monday	ET4251:IoT for Smart Systems
17/04/2023	Monday	PX4291:Electric Vehicles and Power Management
III Semester	Session :	10.00 A.M. to 01.00 P.M.
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	CX4016:Environmental Sustainability
06/04/2023	Thursday	MX4073:Medical Robotics
11/04/2023	Tuesday	PX4011:Grid Integration of Renewable Energy Sources
12/04/2023	Wednesday	PS4351:HVDC and FACTS
13/04/2023	Thursday	PS4071:Energy Management and Auditing
18/04/2023	Tuesday	PS4091:Distributed Generation and Micro Grid
19/04/2023	Wednesday	OCE434:Environmental Impact Assessment
19/04/2023	Wednesday	OBA434:Ethical Management
19/04/2023	Wednesday	OIC431:Blockchain Technologies
19/04/2023	Wednesday	OCE432:Water, Sanitation and Health
19/04/2023	Wednesday	OBA433:Intellectual Property Rights
19/04/2023	Wednesday	OME434:Electric Vehicle Technology
19/04/2023	Wednesday	OME432:Energy Conservation and Management in Domestic Sectors
20/04/2023	Thursday	PX4013:Wind Energy Conversion System
21/04/2023	Friday	PX4012:Renewable Energy Technology
25/04/2023	Tuesday	VE4202:Embedded Automation
27/04/2023	Thursday	PS4093:Smart Grid
II Semester	Session :	2.00 P.M. to 5.00 P.M.
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	PS4072:Energy Storage Technologies
06/04/2023	Thursday	PX4071:Power Quality
10/04/2023	Monday	PX4201:Analysis of Electrical Drives
11/04/2023	Tuesday	PX4202:Special Electrical Machines
12/04/2023	Wednesday	PX4005:Power Electronics for Renewable Energy System
13/04/2023	Thursday	PX4006:Modern Rectifiers and Resonant Converters
17/04/2023	Monday	ET4018:MEMS Design: Sensors and Actuators




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Branch:M.E. VLSI Design

III Semester		
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	CX4016:Environmental Sustainability
06/04/2023	Thursday	MU4153:Principles of Multimedia
10/04/2023	Monday	ET4251:IoT for Smart Systems
11/04/2023	Tuesday	VL4072:CAD for VLSI Design
12/04/2023	Wednesday	ET4072:Machine Learning and Deep Learning
13/04/2023	Thursday	BY4016:IPR, Biosafety and Entrepreneurship
17/04/2023	Monday	VL4073:MEMS and NEMS
17/04/2023	Monday	VL4074:Nanotechnology
17/04/2023	Monday	VL4091:Network on Chip
18/04/2023	Tuesday	DS4151:Digital Image and Video Processing
18/04/2023	Tuesday	VL4009:VLSI Architectures for Image Processing
18/04/2023	Tuesday	VL4011:Adaptive Signal Processing
18/04/2023	Tuesday	VL4010:System Verilog
19/04/2023	Wednesday	OME432:Energy Conservation and Management in Domestic Sectors
19/04/2023	Wednesday	OCE434:Environmental Impact Assessment
19/04/2023	Wednesday	OBA432:Micro and Small Business Management
19/04/2023	Wednesday	OBA433:Intellectual Property Rights
20/04/2023	Thursday	CP4391:Security Practices
21/04/2023	Friday	PX4012:Renewable Energy Technology
24/04/2023	Monday	CU4076:VLSI for Wireless Communication
25/04/2023	Tuesday	MP4251:Cloud Computing Technologies
26/04/2023	Wednesday	VL4351:VLSI Signal Processing
27/04/2023	Thursday	VL4092:Soft Computing and Optimization Techniques
II Semester		
Exam Date	Day	Sub.Code/Name
05/04/2023	Wednesday	VL4291:Low Power VLSI Design
06/04/2023	Thursday	VL4251:Design for Verification using UVM
10/04/2023	Monday	EL4071:Electromagnetic Interference and Compatibility
11/04/2023	Tuesday	VL4252:VLSI Testing
12/04/2023	Wednesday	VL4292:RFIC Design
13/04/2023	Thursday	VL4071:ASIC Design
13/04/2023	Thursday	VL4001:Data Converters
13/04/2023	Thursday	VE4152:Embedded System Design
13/04/2023	Thursday	VL4002:Hardware Software Co Design for FPGA
20/04/2023	Thursday	VL4004:Power Management and Clock Distribution Circuits
20/04/2023	Thursday	II4092:System on Chip
20/04/2023	Thursday	VL4005:Reconfigurable Architectures
20/04/2023	Thursday	AP4095:Signal Integrity for High Speed Design
20/04/2023	Thursday	VL4006:Advanced Wirelss Sensor Networks
III Semester		
Exam Date	Day	Sub.Code/Name
18/04/2023	Tuesday	CP4252:Machine Learning



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TIME TABLE-B.E./B.Tech./B.Arch. DEGREE EXAMINATIONS - NOVEMBER/DECEMBER-2022
(REGULATIONS-2021)

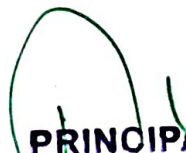
(Except for the candidates admitted in 2022)
CHOICE BASED CREDIT SYSTEM (CBCS)

Branch Name		B.E. Civil Engineering		
emes ter	Subject Code	Subject Name	Exam Date	Session
01	CY3151	Engineering Chemistry	30-DEC-22	A.N.
01	HS3151	Professional English - I	03-JAN-23	A.N.
01	MA3151	Matrices and Calculus	05-JAN-23	A.N.
01	GE3151	Problem Solving and Python Programming	07-JAN-23	A.N.
01	PH3151	Engineering Physics	10-JAN-23	A.N.
02	BE3252	Basic Electrical, Electronics and Instrumentation Engineering	30-DEC-22	F.N.
02	MA3251	Statistics and Numerical Methods	03-JAN-23	F.N.
02	HS3251	Professional English - II	05-JAN-23	F.N.
02	GE3251	Engineering Graphics	07-JAN-23	F.N.
02	PH3201	Physics for Civil Engineering	12-JAN-23	F.N.
03	CE3351	Surveying and Levelling	29-DEC-22	F.N.
03	ME3351	Engineering Mechanics	02-JAN-23	F.N.
03	CE3301	Fluid Mechanics	04-JAN-23	F.N.
03	CE3302	Construction Materials and Technology	06-JAN-23	F.N.
03	MA3351	Transforms and Partial Differential Equations	09-JAN-23	F.N.
03	CE3303	Water Supply and Wastewater Engineering	11-JAN-23	F.N.

Branch Name		B.E. Computer Science and Engineering		
emes ter	Subject Code	Subject Name	Exam Date	Session
01	CY3151	Engineering Chemistry	30-DEC-22	A.N.
01	HS3151	Professional English - I	03-JAN-23	A.N.
01	MA3151	Matrices and Calculus	05-JAN-23	A.N.
01	GE3151	Problem Solving and Python Programming	07-JAN-23	A.N.
01	PH3151	Engineering Physics	10-JAN-23	A.N.
02	BE3251	Basic Electrical and Electronics Engineering	30-DEC-22	F.N.
02	MA3251	Statistics and Numerical Methods	03-JAN-23	F.N.
02	HS3251	Professional English - II	05-JAN-23	F.N.
02	GE3251	Engineering Graphics	07-JAN-23	F.N.
02	CS3251	Programming in C	10-JAN-23	F.N.
02	PH3256	Physics for Information Science	12-JAN-23	F.N.
03	CS3351	Digital Principles and Computer Organization	29-DEC-22	F.N.
03	CS3301	Data Structures	02-JAN-23	F.N.
03	CS3391	Object Oriented Programming	04-JAN-23	F.N.
03	CS3352	Foundations of Data Science	06-JAN-23	F.N.
03	MA3354	Discrete Mathematics	09-JAN-23	F.N.

FN: FORENOON (10.00 A.M. TO 01.00 P.M.)
AN: AFTERNOON (02.00 P.M. TO 05.00 P.M.)




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TIME TABLE-B.E./B.Tech./B.Arch. DEGREE EXAMINATIONS - NOVEMBER/DECEMBER-2022
(REGULATIONS-2021)
(Except for the candidates admitted in 2022)
CHOICE BASED CREDIT SYSTEM (CBCS)

Branch Name		B.E. Electrical and Electronics Engineering		
emes ter	Subject Code	Subject Name	Exam Date	Session
01	CY3151	Engineering Chemistry	30-DEC-22	A.N.
01	HS3151	Professional English - I	03-JAN-23	A.N.
01	MA3151	Matrices and Calculus	05-JAN-23	A.N.
01	GE3151	Problem Solving and Python Programming	07-JAN-23	A.N.
01	PH3151	Engineering Physics	10-JAN-23	A.N.
02	EE3251	Electric Circuit Analysis	30-DEC-22	F.N.
02	MA3251	Statistics and Numerical Methods	03-JAN-23	F.N.
02	HS3251	Professional English - II	05-JAN-23	F.N.
02	GE3251	Engineering Graphics	07-JAN-23	F.N.
02	BE3255	Basic Civil and Mechanical Engineering	10-JAN-23	F.N.
02	PH3202	Physics for Electrical Engineering	12-JAN-23	F.N.
03	CS3353	C Programming and Data Structures	29-DEC-22	F.N.
03	EE3302	Digital Logic Circuits	02-JAN-23	F.N.
03	EE3303	Electrical Machines - I	04-JAN-23	F.N.
03	EE3301	Electromagnetic Fields	06-JAN-23	F.N.
03	EC3301	Electron Devices and Circuits	09-JAN-23	F.N.
03	MA3303	Probability and Complex Functions	11-JAN-23	F.N.

Branch Name		B.E. Electronics and Communication Engineering		
emes ter	Subject Code	Subject Name	Exam Date	Session
01	CY3151	Engineering Chemistry	30-DEC-22	A.N.
01	HS3151	Professional English - I	03-JAN-23	A.N.
01	MA3151	Matrices and Calculus	05-JAN-23	A.N.
01	GE3151	Problem Solving and Python Programming	07-JAN-23	A.N.
01	PH3151	Engineering Physics	10-JAN-23	A.N.
02	BE3254	Electrical and Instrumentation Engineering	30-DEC-22	F.N.
02	MA3251	Statistics and Numerical Methods	03-JAN-23	F.N.
02	HS3251	Professional English - II	05-JAN-23	F.N.
02	GE3251	Engineering Graphics	07-JAN-23	F.N.
02	EC3251	Circuit Analysis	10-JAN-23	F.N.
02	PH3254	Physics for Electronics Engineering	12-JAN-23	F.N.
03	CS3353	C Programming and Data Structures	29-DEC-22	F.N.
03	EC3354	Signals and Systems	02-JAN-23	F.N.
03	EC3351	Control Systems	04-JAN-23	F.N.
03	EC3352	Digital Systems Design	06-JAN-23	F.N.
03	MA3355	Random Processes and Linear Algebra	09-JAN-23	F.N.
03	EC3353	Electronic Devices and Circuits	11-JAN-23	F.N.

FN: FORENOON (10.00 AM TO 1.00 P.M.)
 AN: AFTERNOON (2.00 P.M. TO 5.00 P.M.)



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Reg. No. :

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Question Paper Code : 70069

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Second Semester

Computer Science and Engineering

CS 3251 — PROGRAMMING IN C

(Common to Computer and Communication Engineering/Information Technology)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the various types of operators?
2. What is the use of preprocessor directive?
3. Declare a float array of size 5 and assign 5 values to it.
4. Sort the following elements using selection sort method 23,55,16,78,2.
5. How is pointer arithmetic done?
6. Which is better to use? Macro or function. Justify your answer.
7. What is meant by structure definition?
8. Define self-referential data structure.
9. Why are files needed?
10. Give an example for fseek().


PART B — (5 × 16 = 80 marks)

11. (a) Explain the storage classes in 'C' with suitable examples.

Or

- (b) Explain the looping statement in 'C' with suitable examples.




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12. (a) (i) Write a C program to multiply two matrices (2D array) by getting input from the user. (8)
(ii) Write a C program to find scaling of two matrices (2D array) which will be entered by a user. (8)

Or

- (b) (i) Write a C program to find determinant of a matrix (2D array) which will be entered by a user. (8)
(ii) Write a C program for matrix transpose. (8)
13. (a) (i) Classify the function prototypes with suitable examples. (8)
(ii) Write a C program to design the scientific calculator using built-in functions. (8)

Or

- (b) (i) Explain the concept of pass by value and pass by reference. Write a C program to swap the content of two variables using pass by reference. (8)
(ii) Explain about pointers and write the use of pointers in arrays with suitable example. (8)
14. (a) What is a structure? Create a structure with data members of various types and declare two structure variables. Write a program to read data into these and print the same. Justify the need for structured data type.

Or

- (b) Write a C program to create mark sheet for students using self-referential structure.
15. (a) (i) Write a C program to get name and marks of 'n' number of students from user and store them in a file. (8)
(ii) Write a C program to read name and marks of 'n' number of students from user and store them in a file. If the file previously exists then append the information into the existing file. (8)

Or

- (b) (i) Write a C program to write all the members of an array of structures to a file using fwrite(). Read the array from the file and display on the screen. (8)
(ii) Describe command line arguments with example C program. (8)



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70069

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Office of the Controller of Examinations
Pre- Examination Monitoring System

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- ASSESSMENT
- EXAM RESULTS
- ELECTIVE
- GRUWANCE

[Print](#)

Result for Nov. / Dec. Examination,2023

Register Number :	112420104014		
Name :	LOGESHWARAN G		
Branch :	B.E. Computer Science and Engineering		
Semester	Subject Code	Grade	Result
07	CS8083	B+	PASS
07	CS8711	A+	PASS
07	CS8791	B+	PASS
07	CS8792	A	PASS
07	IT8761	O	PASS
07	MG8591	A	PASS
07	OBM752	A+	PASS
07	SB8051	O	PASS



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Engineering and Technology,
Thirupachur, Thiruvallur - 631 203

Legends

Disclaimer. The result published in this website is provisional only. NIC or O/o CoE, AU are not responsible for any inadvertent error that may have crept in the data / results being published on the Net. This is being published on the Net just for immediate information to the examinees. The Final Mark Sheets issued by the University should only be treated authentic & final in this regard. These Provisional Results will be considered by the University, further, only based on DOTE approval.



ANNA UNIVERSITY :: CHENNAI - 600 025
OFFICE OF THE CONTROLLER OF EXAMINATIONS
Abstract of Photocopies required & Fees Collected
APRIL / MAY EXAMINATION, 2023- EXAMINATIONS

PC

Inst Code & Name : 1124 - SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY

112421106031 SURENHIRAN M K	2	600.00
112421106311 DEEPIKA R	1	300.00
112421106314 ESHWARAN M	5	1500.00
No. of Students :12	No. of Subjects :25	Total : 7500.00

Branch Code / Name : 114 : B.E. Mechanical Engineering University : AUC

Register No.	Name of the Student	No. of Subjects	Fees In Rs.
112421114004 JANAKIRAMAN V		1	300.00
112421114370 RISHI RAJAN R		1	300.00
112421114403 TAMILSELVAN T		2	600.00
No. of Students :3	No. of Subjects :4	Total : 1200.00	

Branch Code / Name : 631 : M.B.A University : AUC

Register No.	Name of the Student	No. of Subjects	Fees In Rs.
112421631001 AARTHI S		1	300.00
112421631020 CHITTIBABU M		2	600.00
112421631116 VIKAAS S V		2	600.00
No. of Students :3	No. of Subjects :5	Total : 1500.00	

Total No. of Students: 27 Total No. of Subjects : 52 Grand Total : 15600.00

The Followings are Enclosed.

i. Obtaining Photocopies of answer book applications received from the students: 27

ii. DD No. Rtus Federal Bank, dated 13/9/23 drawn on (Bank)
Rtus: no: FDR/LH 8256076036 for Rs.15600.

Dt: 13.9.23

College Seal

Encl : As above.

To

The Controller of Examination
Thirupachur
Pin : 631 203



M. Suresh Kumar 13/9/23
Signature of Principal i/c

Name : Dr. L. Palani

Date : 13.9.23
PRINCIPAL



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OFFICE OF THE CONTROLLER OF EXAMINATIONS
 Abstract of Photocopies required & Fees Collected
 APRIL / MAY EXAMINATION, 2023- EXAMINATIONS

PC

Inst Code & Name : 1124 - SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY

Branch Code / Name : 103 : B.E. Civil Engineering University : AUC

Register No.	Name of the Student	No. of Subjects	Fees in Rs.
112421103001	JAYA PRAKASH B S		
112421103314	SANTHOSH KUMAR S	2	600.00
No. of Students :2		4	1200.00
		No. of Subjects :6	Total : 1800.00

Branch Code / Name : 104 : B.E. Computer Science and Engineering University : AUC

Register No.	Name of the Student	No. of Subjects	Fees in Rs.
112421104007	ARVIND SOCKALINGAM S P		
112421104033	MOMEENA S J	3	900.00
112421104049	SRIKANTH E	1	300.00
No. of Students :3		1	300.00
		No. of Subjects :5	Total : 1500.00

Branch Code / Name : 105 : B.E. Electrical and Electronics Engineering University : AUC

Register No.	Name of the Student	No. of Subjects	Fees in Rs.
112421105002	DILLI RANI S		
112421105312	BANUCHANDAR B	1	300.00
112421105316	ELAVARASAN E	3	900.00
112421105319	GANESHKUMAR H	1	300.00
No. of Students :4		2	600.00
		No. of Subjects :7	Total : 2100.00

Branch Code / Name : 106 : B.E. Electronics and Communication Engineering University : AUC

Register No.	Name of the Student	No. of Subjects	Fees in Rs.
112421106006	DAKSHNAMOORTHY B		
112421106007	DEEPIKA P	1	300.00
112421106008	ESWARI S	2	600.00
112421106017	KAVIYARASU U	2	600.00
112421106025	PAVITHRA P	2	600.00
112421106026	PREETHI P	3	900.00
112421106027	RAMYA S	3	900.00
112421106028	RANJANI P	2	600.00
112421106030	SASIKIRAN	1	300.00
		2	300.00



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Provisional Results of April / May Examination,2023(Reval./Photo).

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Inst.Code/Name : 1124 - SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY

Semester No. : 04

DATE OF PUBLICATION :DD-MM-YYYY

Branch : 106-B.E. Electronics and Communication Engineering

Reg Number	Subject Code ->	EC3451	EC3452	EC3491	GE3451
Reg Number	Stud. Name	Grade	Grade	Grade	Grade
112421106006	DAKSHNAMOORTHY B		NC		
112421106007	DEEPIKA P			NC	
112421106008	ESWARI S	NC			
112421106017	KAVIYARASU U	NC		NC	
112421106025	PAVITHRA P		NC	NC	
112421106026	PREETHI P	NC		NC	
112421106027	RAMYA S	B+		NC	
112421106028	RANJANI P			NC	
112421106030	SASIKIRAN R	B+			
112421106031	SURENDRHIRAN M K	B+		NC	
112421106311	DEEPIKA R		B+		
112421106314	ESHWARAN M	NC	NC	NC	NC



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W - Withdrawal I - Inadequate Attendance

WH1 - Withheld for Suspected Malpractice WH(others) - Withheld for want of Clarification,approval,etc.

16-12-2023

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Provisional Results of April / May Examination,2023(Reval/Photo).

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Inst.Code/Name : 1124 - SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY

Semester No. : 06

DATE OF PUBLICATION : DD-MM-YYYY

Branch : 106-B.E. Electronics and Communication Engineering

Reg Number	Stud Name	Grade	Grade
112420106356	SANDHYA S	NC	B



A handwritten signature in blue ink, appearing to be "S. Venkateswara", written over the printed name of the Principal.

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W - Withdrawal I - Inadequate Attendance

WH1 - Withheld for Suspected Malpractice WH(others) - Withheld for want of Clarification,approval,etc.

16-12-2023

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