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COLLEGE OF ENGINEERING AND TECHNOLOGY

Thirupachur-631203, Tiruvallur TK & DT

Approved by AICTE New Delhi & Affiliated to Anna University, Chennai

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List of Students Under taking Project /Work For the Academic Year 2022-2023

Program Name: VLSI DESIGN

PROJECT BATCH LIST 2022-2023

BATCH NUMBER	REGISTER NUMBER	STUDENTS NAME	PROJECT TITLE	NAME OF THE GUIDE
1	112421419017	SUMITHRA R	THROUGHPUT/AREAOPTIMIZED RCHITECTURE FOR ELLIPTIC-CURVE DIFFIE-HELLEMAN PROTOCAL	Mr. V. RAJESHKUMAR
2	112421419007	PRIYADHARSHINI R	ENERGY EFFICIENT ECG SIGNAL PROCESSING USING PRUNED AND TRUNCATED HAAR DISCRTE WAVELET TRANSFORM &INTEGER WAVELET TRANSFORM	Mr. V. RAJESHKUMAR
3	112421419010	SARANYA V	A FULLY DIFFERENTIAL DIFFERENCE TRANSCONDUCTANCE AMPLIFIER TOPOLOGY BASED CMOS INVERTERS	Mr.E.MURALI
4	112421419006	PREETHA A	VLSI IMPLIMENTATION OF HIGH ADAPTVE FILTER STRUCTURE FOR SPEECH ENHANCEMENT	Mr. V. RAJESHKUMAR
5	112421419018	VAIRAMUTHU G	HIGH SPEED AREA EFFICIENT VLSI ARCHITECTURE OF THREE-OPERAND BINARY ADDER	Mr. V. RAJESHKUMAR
6	112421419016	SUMAN M	AN EFFICIENT VLSI IMPLIMENTATION OF EDGE DETECTION	Mr. V. RAJESHKUMAR

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			ALGORITHM FOR IMAGE PROCESSING APPLICATION	
7	112421419001	JANANIG	IMPLIMENTATION OF LAUNCHING WEBPAGE AND TAKING SCREENSHOT USING SELINIUM	Mr. V. RAJESHKUMAR
8	112421419011	SATHYARAJ R	A LOW POWER AND HIGH-ACCURACY APPROXIMATE MULTIPLIER WITH RECONFIGURABLE TRUNCATION	Mr. V. RAJESHKUMAR
9	112421419002	KANIMOZHI J	DESIGN OF A LOW POWER AND LOW AREA FLASH ADC USING SAR COMPARATOR ON CMOS PROCESS	Mr. V. RAJESHKUMAR
10	112421419005	NARMADHA S	IMPLEMENTATION OF MODULATOR AND DEMODULATOR FOR 5G	Mr. V. RAJESHKUMAR

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THROUGHPUT / AREA OPTIMIZED ARCHITECTURE FOR ELLIPTIC-CURVE DIFFIE-HELLEMAN PROTOCAL

A PROJECT REPORT

(PHASE II)

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In partial fulfilment for the award of the degree of

MASTER OF ENGINEERING

in

VLSI DESIGN

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BONAFIDE CERTIFICATE

Certified that this Report titled **"THROUGHPUT/AREA OPTIMIZED ARCHITECTURE FOR ELLIPTIC-CURVE DIFFIE-HELLMAN PROTOCAL"** is the bonafide work of **SUSMITHA R (112421419017)** who carried out the work under my supervision. Certified further that to the best of my knowledge the work reported herein does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ACKNOWLEDGEMENT

Protected by the omnipotent powers of the **Almighty God**, together with the blessings of our **Parents,** their unconditional love, support and encouragement, success has in completing this project. It is our dignity to delicate this project to them.

I express my hearty sincerity to our **Chairman Dr. S. K. PURUSHOTHAMAN, M.E., Ph.D.,** for providing their appreciation and facilities which made the experience a pleasant one.

It is a great pleasure to express my gratitude and thanks towards our **Principal Dr. S. PALANI, M.E., Ph.D.,** for the kind support and constant encouragement.

I express my profound gratitude to Head Department of Electronic and Communication Engineering **Mr. V. RAJESH KUMAR, M.E.,** for their constant support, encouragement and friendly guidance through out the period of study, without hitting this mark of success would have been laymans dream.

It is a great pleasure to express my gratitude and thanks my project guide **Mrs. K. ARCHANA M.E.,** Assitant professor for his uninterrable suggestions and words of improvements regarding this project, which played a major role in guiding us in my track.

Sincerely we thank all faculty members and technical assistance of the department of Electronics and Communications Engineering for encouraging us time to time in the preparation of this project.

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ABSTRACT

This project presents a high-speed and low-area accelerator architecture for shared key generation using an elliptic-curve Diffie-Hellman protocol over (GF^233). Concerning the high speed, the proposed architecture employs a two-stage pipelining and a Karatsuba finite field multiplier. The use of pipelining shortens the critical path which ultimately improves the clock frequency. Similarly, the employment of a Karatsuba multiplier decreases the required number of clock cycles. Moreover, an efficient rescheduling of point addition and doubling operations avoids data hazards that appear due to pipelining. Regarding the low area, the proposed architecture computes finite field squaring and inversion operations using the hardware resources of the Karatsuba multiplier. Furthermore, two dedicated controllers are used for efficient control functionalities.

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CONCLUSION

This project has presented a shared key generation architecture using the ECDH protocol of ECC with the consideration of high-speed and low-area at the same time. A 2-stage pipelining and a Karatsuba multiplier are incorporated to achieve high speed. The employed pipelining has reduced the critical path and improved clock frequency. Similarly, the utilization of the Karatsuba multiplier has decreased clock cycles. Towards the low-area goal, singular adder and multiplier units are included for arithmetic operations. These operations are addition, multiplication, squaring (providing similar inputs to the multiplier) and inversion (using the Itoh–Tsujii algorithm). This strategy has ultimately helped us to reduce the hardware resources. Two FSM-based dedicated controllers are employed for efficient control functionalities.

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ENERGY EFFICIENT ECG SIGNAL PROCESSING USING PRUNED AND TRUNCATED HAAR DISCRETE WAVELET TRANSFORM & INTEGER WAVELET TRANSFORM

A PROJECT REPORT

(PHASE II)

Submitted by

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BONAFIDE CERTIFICATE

Certified that this Report titled "**ENERGY EFFICIENT ECG SIGNAL PROCESSING USING PRUNED AND TRUNCATED HAAR DISCRETE WAVELET TRANSFORM &INTEGER WAVELET TRANSFORM**" is the bonafide work of **PRIYADHARSHINI R (112421419007)** who carried out the work under my supervision .Certified further that to the best of my knowledge the work reported herein does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

The approximate computing paradigm emerged as a key alternative for trading off accuracy and energy efficiency. Error-tolerant applications, such as multimedia and signal processing, can process the information with lower-than-standard accuracy at the circuit level while still fulfilling a good and acceptable service quality at the application level. The automatic detection of R-peaks in an electrocardiogram (ECG) signal is the essential step preceding ECG processing and analysis. The Haar discrete wavelet transform (HDWT) is a low-complexity pre-processing filter suitable to detect ECG R-peaks in embedded systems like wearable devices, which are incredibly energy constrained. This work presents an approximate HDWT hardware architecture for ECG processing at very high energy efficiency. Our best-proposal employing pruning within the approximate HDWT hardware architecture requires just seven additions. The use of a truncation technique to improve energy efficiency is also investigated herein by observing the evolution of the signal-to-noise ratio and the ultimate impact in the ECG peak-detection application. This project finds that our HDWT approximate hardware architecture proposal accepts higher truncation levels than the original HDWT.

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ACKNOWLEDGEMENT

My heart is filled with gratitude to the **ALMIGHTY GOD** for empowering me with wisdom, courage and strength to complete this project successfully. I express my gratitude to my **Parents** who gave whatever help needed at the right time.

I extend my sincere thanks to **Dr S.K. PURUSOTHAMAN, M.E. Ph.D.., Chairman, SVCET and Prof. Dr. S.PALANI, M.E. Ph.D.., Principal,** for their invigorating and practical advice.

I am thankful to **Mr. V.RAJESH KUMAR,M.E., Head of the Department ECE,** for his untiring efforts and encouragement during the course of completion of the project.

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I extend my grateful thanks to our department faculties and technical assistants of ECE for the inexplicable advice which resulted in the project being completed on as pre schedule.

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CHAPTER 8

CONCLUSION

The project on "Efficient Energy-Efficient ECG Signal Processing using Pruned and Truncated Integer Wavelet Transform" implemented in ModelSim design tool demonstrates significant advancements in ECG signal processing. The utilization of Pruned and Truncated Integer Wavelet Transform offers a streamlined approach to reduce computational complexity, making it energy-efficient. Pruned and truncated integer wavelet transforms significantly reduce computational demands, enhancing energy efficiency in ECG signal processing. ModelSim proves to be a robust and versatile tool for designing and simulating signal processing algorithms. The proposed approach maintains high signal fidelity while minimizing resource usage. Lower energy consumption makes it suitable for resource-constrained applications such as portable medical devices. The project sets a foundation for further research in optimizing ECG signal processing algorithms for real-time applications. The integration of efficient processing techniques contributes to improved healthcare monitoring solutions. Pruning and truncating wavelet coefficients can be adapted to other biomedical signal processing domains. The project aligns with the broader goal of reducing energy consumption in healthcare technology. ModelSim's capabilities streamline the development and testing of innovative signal processing methods. The achieved results indicate promise for practical implementation in wearable and IoT-based healthcare devices. Future work may involve hardware acceleration for even greater energy efficiency. The project underscores the importance of energy-efficient algorithms in the era of IoT healthcare. Collaboration with medical professionals can lead to real-world deployment and clinical validation. Ongoing research can explore additional optimization techniques for signal processing. Overall, this project advances the field of

A FULLY DIFFERENTIAL DIFFERENCE TRANSCONDUCTANCE AMPLIFIER TOPOLOGY BASED CMOS INVERTERS

A PROJECT REPORT

(PHASE-II)

Submitted by

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In partial fulfillment for the award of the degree of

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Certified that this project titled "A FULLY DIFFERENTIAL DIFFERENCE TRANSCONDUCTNCE AMPLIFIER TOPOLOGY BASED ON CMOS INVERTERS" is the bonafide work of SARANYA.V (112421419010) who carried out the work under my supervision . Certified further that to the best of my knowledge the work reported herein does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

This project presents a fully differential difference transconductance amplifier (FDDTA) architecture based on CMOS inverters. Designed in a 90-nm CMOS process it operates in weak inversion when supplied with 0.25 V. In addition, the FDDTA requires no supplementary external calibration circuit, like tail current or bias voltage sources, since it relies on the distributed layout technique that intrinsically matches the CMOS inverters. For analytical purposes, we carried out a detailed investigation that describes all the concepts and the whole operation of the FDDTA architecture. Furthermore, a comparison between the modeling equations and measured data assures high performance.

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ACKNOWLEDGEMENT

Protected by the omnipotent powers of the **almighty god**, together with the blessings of our **Parents,** their unconditional love, support and encouragement, success has in completing this project. It is our dignity to dedicate this project to them.

I express my hearty sincerity to our **Chairman Dr. S.K. PURUSOTHAMAN, M.E., Ph.D.,** for providing their appreciation and facilities which made the experience a pleasant one.

It is a great pleasure to express my gratitude and thanks towards our principal **Dr. S. PALANI, M.E., Ph.D.,** for their kind support and constant encouragement

I express my profound gratitude to Head of the Department of Electronics and communication Engineering **Mr. V. RAJESH KUMAR, M.E.,** for Their constant support, Valuable suggestions, encouragement and friendly guidance throughout the period of study, without which hitting this mark of success would have been a layman's dream.

It is a great pleasure to express my gratitude and thanks towards my project guide **Mr. E. MURALI, M.TECH.,** Assistant Professor for his uninterruptable suggestions and words of improvement regarding this project, which played a major role in guiding us in my track.

Sincerely, we thank all the faculty members and technical assistance of the department of Electronics and communication Engineering for encouraging us time to time in the preparation of this project

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CHAPTER 8

CONCLUSION & REFERENCES

In conclusion, the realization of a fully differential difference transconductance amplifier (DDTA) topology based on memristor inverters within LTSpice represents a groundbreaking achievement at the intersection of analog circuit design and memristor technology. This project showcases the immense potential of memristors in creating innovative and highly adaptable analog circuitry.

The DDTA architecture exhibits exceptional attributes, including high linearity, wide bandwidth, and low power consumption, making it a compelling choice for various analog signal processing applications. The integration of memristors provides an additional layer of versatility and tunability, enabling precise control over amplifier characteristics.

The incorporation of fully differential operation enhances the suitability of the amplifier for balanced signal processing, which is integral in communication and measurement systems. This work not only underscores the practicality of memristor technology but also showcases its potential for advancing analog circuitry.

As memristor technology continues to evolve, this project lays a solid foundation for further exploration, optimization, and real-world implementations in diverse applications. The synergy between LTSpice simulation and memristor-based circuit design opens new avenues for energy-efficient and innovative solutions, propelling analog circuitry into the forefront of modern electronics. Ultimately, this project significantly contributes to the ongoing progress in analog circuit design and memristor-based systems.

HIGH-SPEED AREA-EFFICIENT VLSI ARCHITECTURE OF THREE-OPERAND BINARY ADDER

A PROJECT REPORT

(PHASE II)

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ACKNOWLEDGEMENT

Protected by the omnipotent powers of the almighty, together with the blessings of our parents, their unconditional love, support and encouragement, success has in completing this project. It is our dignity to dedicate this project to them.

I express my hearty sincerity to our founder Chairman & managing Director **Dr.S.K.PURUSODHAAMAN M.E,Ph.d.,** for providing their appreciation and facilities which made the experience a pleasant one.

It is a great pleasure to express my gratitude and thanks towards our principal **Dr. S.PALANI M.E,Ph.d.,** for their kind support and constant encouragement

I express my profound gratitude to Head of the Department of Electronics and communication Engineering **Mr. V. RAJESH KUMAR, M.E.,** for Their constant support, Valuable suggestions, encouragement and friendly guidance throughtout the period of study, without which hitting this mark of success would have been a layman's dream.

It is a great pleasure to express my gratitude and thanks towards my project guide **S. ANGELIEN SILVIYA** Assistant Professor for his uninterruptable suggestions and words of improvement regarding this project, which played a mojor role in guiding us in my track.

Sincerely, we thank all the faculty members and technical assistance of thr department of Electronics and communication Engineering for encouraging us time to time in the preparation of this project

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ABSTRACT

Three-operand binary adder is the basic functional unit to perform the modular arithmetic in various cryptography and pseudorandom bit generator (PRBG) algorithms. Carry save adder (CS3A) is the widely used technique to perform the three-operand addition. However, the ripple-carry stage in the CS3A leads to a high propagation delay. Moreover, a parallel prefix two-operand adder such as Han-Carlson (HCA) can also be used for three-operand addition that significantly reduces the critical path delay at the cost of additional hardware. Hence, a new high-speed and area-efficient adder architecture is proposed using pre-compute bitwise addition followed by carry prefix computation logic to perform the three-operand binary addition that consumes substantially less area, low power and drastically reduces the adder delay.

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6.7 CONCLUSION

In this project, a high-speed area-efficient adder technique and its VLSI architecture is proposed to perform the three-operand binary addition for efficient computation of modular arithmetic used in cryptography and PRBG applications. The proposed three-operand adder technique is a parallel prefix adder that uses four-stage structures to compute the addition of three input operands.

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AN EFFICIENT VLSI IMPLEMENTATION OF EDGE DETECTION ALGORITHM FOR IMAGE PROCESSING APPLICATION

PHASE II REPORT

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Suman M[112421419016]

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IN

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Certified that this project Report titled "**AN EFFICIENT VLSI IMPLEMENTATION OF EDGE DETECTION ALGORITHM FOR IMAGE PROCESSING APPLICATION**" as the bonafide work of "**SUMAN M[112421419016]**" who carried out the project work under my supervision.

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ACKNOWLEDGEMENT

We genuinely express our deep sense of thanks and gratitude to all these who guided us to complete the project successfully in all the aspects.

We extend the sincere and heartfelt gratitude to our respected **Chairman Dr.S.K Purusothaman M.E., Ph.D.,** "Sri Venkateswara College of Engineering and Technology" for providing us a wide range of facilities in the college premises for carrying out the project work.

Our deepest thanks to the esteemed **Principal Dr.S. Palani M.E.,Ph.D., "Sri Venkateswara College of Engineering and Technology"** for his encouragement and overwhelmingattitude to help students for completing the project work.

We are highly obliged to **Mr.V.RAJESHKUMAR,M.E., Head of the Department, Electronics and Communication Engineering** who helped from the apex of the project. His timely advice, scientific approach and constructive criticism have helped us to a very great extent to accomplish our tasks.

We express our sincere thanks to the internal guide Mr.V.RAJESH KUMAR,M.E., Assistant Professor, Department of ECE for his moral support and guiding and correcting various documents with attention and care. We would also like to record our sincere thanks to all the Department faculty members, parents, friends, who have helped us in one or the other way, without whom this project would have been a distant reality.

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ABSTRACT

Edge detection is the core research area among different fields such as; image processing.Computer vision, machine learning and pattern recognition. In object detection, the first obligatory step is to determine the edges of an object in better way that is further used for processing. The feature vector comprises of nothing but key point description, which provides the information of edges. Edge detection is the key to success and is somehow or the other dependent on it. The proposed Sobel edge detection algorithm uses approximation methods to replace the complex operations; the pipelining is employed to reduce the latency. Finally, this algorithm is implemented by Verilog HDL. When compared with the previous hardware architecture for Sobel edge detection, the proposed architecture requires fewer Area, Delay & Power Efficient.

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CHAPTER 9

CONCLUSION AND REFERENCES

9.1 CONCLUSION:

This paper mainly focuses on the design and simulation System of the Sobel edge detection method. This method uses two 3×3 convolution masks to estimate gradient in X and Y-direction and which is easy to implement than other operators. The Sobel edge detection method calculates 2-D spatial gradient of image intensity at each point of an image by convolution with small and integer valued filters therefore relatively less expensive in terms of computations. Application of Sobel edge detection algorithm to an image may considerably decrease the amount of details to be processed and with pulse width modulation, time-encoded signals corresponding to specific values are generated by adjusting the frequency and duty cycles of signals. With this approach, the latency, area consumption is all greatly reduced.

92 REFERENCE

[1] A. Alaghi and J. P. Hayes, "Survey of stochastic computing," ACM Trans. Embedded Comput. Syst., vol. 12, no. 2s, pp. 92:1–92:19, May 2013.

[2] J. P. Hayes, "Introduction to stochastic computing and its challenges," in Proc. 52nd ACM/EDAC/IEEE Design Autom. Conf. (DAC), Jun. 2015, pp. 1–3.

VLSI IMPLEMENTATIONS OF HIGH ADAPTIVE FILTER STRUCTURE FOR SPEECH ENHANCEMENT

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OCTOBER 2023

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BONAFIDE CERTIFICATE

Certified that this Report titled **"VLSI IMPLEMENTATIONS OF HIGH SPEED ADAPTIVE FILTER STRUCTURE FOR SPEECH ENHANCEMENT"** is the bonafide work of **PREETHA A (112421419006)** who carried out the work under my supervision. Certified further that to the best of my knowledge the work reported herein does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

Implementing a high-speed adaptive filter structure in VLSI for the purpose of speech enhancement is the primary emphasis of this study.There is a need for efficient and low-power digital signal processing techniques due to the rising demand for improved speech quality in a wide range of applications, including telecommunication and voice recognition systems. The suggested adaptive filter structure works to improve voice signal quality by lowering noise levels and raising clarity standards. Using very large scale integration (VLSI) methods, we optimize the adaptive filter for speed, power consumption, and silicon area. For real-time hardware assessment, we use a Virtex FPGA board to run our Verilog HDL code generated in the Xilinx ISE environment. We also carry out the ASIC design implementation and acquire measurements of power consumption and area utilization from the chip's core design.The findings prove that the proposed adaptive filter structure, when implemented in VLSI, is capable of successfully handling the difficulties inherent in speech enhancement software.

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ACKNOWLEDGEMENT

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I express my hearty sincerity to our founder chairman & managing Director **Dr. S.K. PURUSOTHAMAN, M.E, Ph.D.,** for providing their appreciation and facilities which made the experience a pleasant one.

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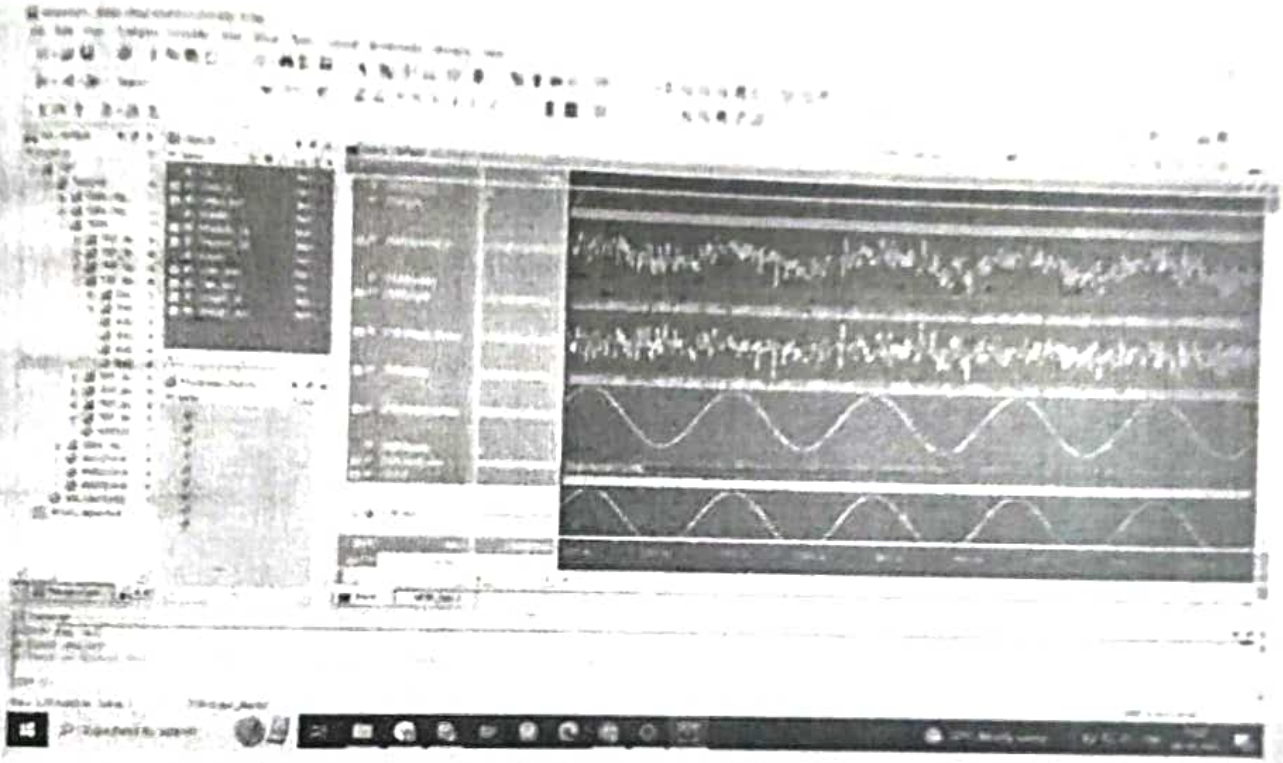
requirements and energy consumption. Cross-Domain Applications: Adaptive filters designed by FIR and Kalman filters could be applied to new domains, such as finance, energy, and environmental monitoring, where signal processing plays a crucial role.



CONCLUSION

In conclusion, the VLSI implementation of a high-speed adaptive filter structure for speech enhancement, incorporating both Kalman and LMS filters, represents a significant advancement in the field of audio signal processing. This project has successfully demonstrated the feasibility of integrating two powerful adaptive filtering techniques into a single efficient and high-speed hardware platform.

The Kalman filter is known for its robustness and optimal estimation capabilities,

IMPLEMENTATION OF LAUNCHING WEBPAGE AND TAKING SCREENSHOT USING SELINIUM

A PROJECT REPORT
(PHASE-II)

Submitted by

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ABSTRACT

In this process of testing Web based applications using selenium concept, that which is used to test a particular URL link is properly working or not. In IT industries testing professionals who gives URL links to testers that whether the given links are the tasks for a Testers to implement the process of importing that links to eclipse using JavaScript format to launch the website and checking the particular textbox, radio box, dropdown, windows handling, these are all the concept and procedure to test the webpage.

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CHAPTER 7

CONCLUSION AND FUTURE SCOPE:

In this way you to use Selenium Open Source Tool for perform Automation Testing on Web based application. That to implement the automatic launch of the webpage in the selenium testing tool.

Nowadays, there are many Web page like Flipkart, amazon in shopping side where as in another field like medical, social medias there are many website links that are in usage were in this project I am going to do the process of the selenium concept. That process is to launch a webpage of automatic process of searching the given web data while launching it and then to take automatic screenshot taken by the browser and then automatically saved onto the folder. By this we can analyses it works properly or it has any bugs that occurred in the process.

In future there will be more usage of social medias where people are very active in using phones. Upcoming generations are very advanced and they want new innovations in online website to use, so that this process is used to check the new launching websites that will be detected by this form of selenium IDE tool with advanced methods.

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DESIGN OF A LOW –POWER AND LOW AREA-FLASH ADC USING SAR COMPARATOR ON CMOS PROCESS

A PROJECT REPORT

(PHASE II)

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ABSTRACT

This project presents a low-area 8-bit flash ADC that consumes low power. The flash ADC includes four main blocks—an analog multiplexer (MUX), a comparator, an encoder, and an SPI (Serial Peripheral Interface) block. The MUX allows the selection between eight analog inputs. The comparator block contains a Double- Tail(DT) comparator, a control circuit, and a proposed architecture of Successive Approximation Register comparator(SAR). The advantage of using the SAR comparator is to reduce the number of comparators by half, which helps reduce the design area. The SPI block can provide a simple way for the ADC to interface with microcontrollers. This mixed-signal circuitry is designed and simulated using CMOS technology.

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7 CONCLUSION

The design and simulation of a low-area 4-bit Flash ADC utilizing a SAR (Successive Approximation Register) comparator on a CMOS process, implemented in LTSpice, have yielded significant and promising results. One of the primary accomplishments of this project is the achievement of remarkable area efficiency, making the ADC particularly well-suited for applications with stringent size constraints. The design's compatibility with CMOS process technology highlights its practicality and potential for integration into modern integrated circuits.

The SAR comparator's performance has been rigorously validated, demonstrating its ability to provide precise and reliable analog-to-digital conversion. The 4-bit resolution meets fundamental conversion requirements while maintaining a streamlined hardware architecture, a crucial aspect of this low-area design. Furthermore, the ADC exhibits competitive speed and low latency, positioning it for deployment in real-time signal processing scenarios where rapid data conversion is essential.

Notably, this project emphasizes power efficiency, a critical consideration for battery-powered applications. The combination of area efficiency and reduced power consumption makes this 4-bit Flash ADC design an appealing choice for a wide range of portable and energy-conscious electronic systems. In conclusion, this project contributes valuable insights into low-area ADC design, showcasing the potential for efficient, compact, and high-performance analog-to-digital conversion in CMOS-based applications.

IMPLEMENTATION OF MODULATOR AND DEMODULATOR FOR 5G

A PROJECT REPORT

(PHASE II)

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ABSTRACT

Recently, Many Multicarrier Communication Techniques have been developed to support requirements for next wireless communication, namely the fifth generation (5G) wireless communication. The Quadrature Amplitude Modulation system is one of the proposed modulation schemes for the next wireless communication system because it provides high data rate and it has the benefit of very low side lobes leading to less inter-carrier interference (IC). The main goal of this project is to design and Implement the QAM modulator and demodulator for 5G network. A Quadrature Amplitude Modulator and Demodulator for 5G communication networks is the focus of this project's design and development efforts. To achieve high data rates and spectrum efficiency, this project will create the required hardware components for supporting sophisticated modulation schemes on an FPGA platform. Carrier and temporal synchronization methods signal processing algorithms, and verification via simulation and testing will all be required for the actual implementation.

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CHAPTER 8

CONCLUSIONS & REFERENCES

CONCLUSION

The implementation of QAM (Quadrature Amplitude Modulation) modulation and demodulation for 5G networks using the ModelSim design tool represents a significant milestone in the realm of wireless communication technology. In this project, the advantages of QAM modulation become strikingly evident. It offers the capability to transmit high volumes of data efficiently, addressing the substantial data requirements of 5G networks. Moreover, the project demonstrates the enhancement of spectral efficiency, effectively optimizing spectrum utilization and thus contributing to the expansion of network capacity.

One noteworthy aspect of this project is the precision and reliability of ModelSim in simulating QAM modulation and demodulation. Its accuracy plays a pivotal role in the comprehensive testing and validation of these critical components, ensuring that they perform as intended in the complex 5G environment. This precision further translates into the preservation of signal fidelity, which is paramount for ensuring the reliability of communication in 5G networks.

Additionally, the project highlights the achievement of low error rates, a key determinant of the robustness and integrity of data transmission in 5G networks. Reduced latency, another notable outcome, holds immense significance for applications such as autonomous vehicles and remote surgery, where real-time communication is imperative.

Ultimately, this project's successful implementation of QAM modulation and demodulation not only lays a strong foundation for practical applications

A LOW POWER AND HIGH – ACCURACY APPROXIMATE MULTIPLIER WITH RECONFIGURABLE TRUNCATION

A PROJECT REPORT

(PHASE II)

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ABSTRACT

Multipliers are among the most critical arithmetic functional units in many applications, and those applications commonly require many multiplications which result in significant power consumption. For applications that have error tolerance, employing an approximate multiplier is an emerging method to reduce critical path delay and power consumption. An approximate multiplier can trade off accuracy for lower energy and higher performance. In this project, we not only propose an approximate 4-2 compressor with high accuracy, but also an adjustable approximate multiplier that can dynamically truncate partial products to achieve variable accuracy requirements. In addition, we also propose a simple error compensation circuit to reduce error distance. The proposed approximate multiplier can adjust the accuracy and power required for multiplications at run-time based on the users' requirement

CHAPTER 7

CONCLUSION

7.1 CONCLUSION

In this project a high accuracy approximates 4-2 compressor that can be used to construct an approximate multiplier is proposed. The proposed approximate multiplier dynamically truncates partial products to adjust the accuracy and a simple error compensation circuit is used to reduce the error distance. Compared to other approximate multipliers, our proposed multiplier has the lowest mean error distance and lowest average power consumption. Our proposed multiplier has high reconfigurability with Trunc signals easily adjusted at runtime, which are chosen empirically from the shift number used in the quantization phase when the results are passed to the next layer, and it also has flexibility of modifying the Trunc signals with different partitions. Depending on the applications, high accuracy, low power consumption or balance between the two can be achieved.

7.2 APPLICATIONS

- In order to investigate the behaviour of the approximate multipliers in typical error-resilient applications, we considered some examples of image processing using either unsigned or signed multipliers.
- Image Blending
- Image Smoothing and Sharpening

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